

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

www.qdzbwx.com

SCHEM, MLB, KEPLER, 2PHASE, D2
FSB, 5/9/2012

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2012-05-09

Page		Contents	Sync	Date
1	1	Table of Contents	D2_KEPLER	01/13/2012
2	2	System Block Diagram	D2_KEPLER	01/13/2012
3	3	Power Block Diagram	D2_KEPLER	01/13/2012
4	4	Revision History	D2_KEPLER	01/13/2012
5	5	BOM Configuration	D2_KEPLER	01/13/2012
6	6	BOM Variants	D2_KEPLER	01/13/2012
7	7	Functional / ICT Test	D2_KEPLER	01/13/2012
8	8	Power Aliases	D2_KEPLER	01/13/2012
9	9	Signal Aliases	D2_KEPLER	01/13/2012
10	10	CPU DMI/PEG/FDI/RSVD	D2_KEPLER	01/13/2012
11	11	CPU CLOCK/MISC/JTAG	D2_KEPLER	01/13/2012
12	12	CPU DDR3 INTERFACES	D2_KEPLER	01/13/2012
13	13	CPU POWER	D2_KEPLER	01/13/2012
14	14	CPU POWER AND GND	D2_KEPLER	01/13/2012
15	16	CPU DECOUPLING-I	D2_SEAN	03/05/2012
16	17	CPU DECOUPLING-II	D2_SEAN	03/05/2012
17	18	PCH SATA/PCIe/CLK/LPC/SPI	D2_KEPLER	01/13/2012
18	19	PCH DMI/FDI/PM/Graphics	D2_KEPLER	01/13/2012
19	20	PCH PCI/USB/TP/RSVD	D2_KEPLER	01/13/2012
20	21	PCH GPIO/MISC/NCTF	D2_KEPLER	01/13/2012
21	22	PCH POWER	D2_CLEAN	03/19/2012
22	23	PCH GROUNDS	D2_KEPLER	01/13/2012
23	24	PCH DECOUPLING	D2_CLEAN	03/19/2012
24	25	CPU & PCH XDP	D2_KEPLER	01/13/2012
25	26	Chipset Support	D2_KEPLER	01/13/2012
26	27	USB HUB & MUX	D2_KEPLER	01/13/2012
27	28	CPU Memory S3 Support	D2_KEPLER	01/13/2012
28	29	DDR3 SDRAM Bank A (1 OF 2)	D2_KEPLER	01/13/2012
29	30	DDR3 SDRAM Bank A (2 OF 2)	D2_KEPLER	01/13/2012
30	31	DDR3 SDRAM Bank B (1 OF 2)	D2_KEPLER	01/13/2012
31	32	DDR3 SDRAM Bank B (2 OF 2)	D2_KEPLER	01/13/2012
32	33	DDR3 Termination	D2_KEPLER	01/13/2012
33	34	DDR3/FRAMEBUF VREF MARGINING	D2_KEPLER	01/13/2012
34	35	X29/ALS/CAMERA CONNECTOR	D2_KEPLER	01/13/2012
35	36	Thunderbolt Host (1 of 2)	D2_KEPLER	01/13/2012
36	37	Thunderbolt Host (2 of 2)	D2_KEPLER	01/13/2012
37	38	Thunderbolt Power Support	D2_KEPLER	01/13/2012
38	44	RIO CONNECTOR	D2_KEPLER	01/13/2012
39	45	SSD CONNECTOR	D2_KEPLER	01/13/2012
40	46	USB 3.0 CONNECTORS	D2_KEPLER	01/13/2012
41	49	SMC	D2_KEPLER	01/13/2012
42	50	SMC Support	D2_KEPLER	01/13/2012
43	51	LPC+SPI Debug Connector	D2_KEPLER	01/13/2012
44	52	SMBUS Connections	D2_KEPLER	01/13/2012
45	53	Voltage & Load Side Current Sensing	D2_SEAN	03/05/2012


Page	Contents	Sync	Date
46	High Side and CPU/AXG Current Sensing	D2_SEAN	03/05/2012
47	Thermal Sensors	D2_SEAN	03/05/2012
48	Fan Connectors	D2_KEPLER	01/13/2012
49	KEYBOARD/TRACKPAD (1 OF 2)	D2_KEPLER	01/13/2012
50	KEYBOARD/TRACKPAD (2 OF 2)	D2_KEPLER	01/13/2012
51	DIGITAL ACCELEROMETER & GYRO	D2_KEPLER	01/13/2012
52	SPI ROM	D2_KEPLER	01/13/2012
53	AUDIO: CODEC/REGULATOR	D2_CARA	03/16/2012
54	AUDIO: HEADPHONE FILTER	D2_CARA	03/16/2012
55	AUDIO: IV SENSE	D2_CARA	03/16/2012
56	AUDIO: IV SENSE FILTER	D2_CARA	03/16/2012
57	AUDIO: SPEAKER AMP	D2_CARA	03/16/2012
58	AUDIO: JACK	D2_CARA	03/16/2012
59	AUDIO: JACK TRANSLATORS	D2_CARA	03/16/2012
60	DC-In & Battery Connectors	D2_KEPLER	01/13/2012
61	PBus Supply & Battery Charger	D2_KEPLER	01/13/2012
62	System Agent Supply	D2_KEPLER	01/13/2012
63	5V / 3.3V Power Supply	D2_KEPLER	01/13/2012
64	1V5R1V35V DDR3 SUPPLY	D2_KEPLER	01/13/2012
65	CPU IMVP7 & AXG VCore Regulator	D2_SEAN	03/05/2012
66	CPU IMVP7 & AXG VCore Output	D2_SEAN	03/05/2012
67	CPU VCCIO (1V0R1V05 S0) POWER SUPPLY	D2_KEPLER	01/13/2012
68	Misc Power Supplies	D2_KEPLER	01/13/2012
69	Power FETs	D2_KEPLER	01/13/2012
70	Power Control 1/ENABLE	D2_KEPLER	01/13/2012
71	KEPLER PCI-E	D2_KEPLER	01/13/2012
72	KEPLER CORE/FB POWER	D2_SEAN	03/05/2012
73	KEPLER FRAME BUFFER I/F	D2_SEAN	03/05/2012
74	1V05 GPU / 1V35 FB POWER SUPPLY	D2_SEAN	03/05/2012
75	GDDR5 Frame Buffer A	D2_SEAN	03/05/2012
76	GDDR5 Frame Buffer B	D2_SEAN	03/05/2012
77	KEPLER EDP/DP/GPIO	D2_SEAN	03/05/2012
78	KEPLER GPIOs,CLK & STRAPS	D2_SEAN	03/05/2012
79	KEPLER PEX PWR/GNDS	D2_SEAN	03/05/2012
80	GFx IMVP VCore Regulator	D2_SEAN	03/05/2012
81	eDP Display Connector	D2_KEPLER	01/13/2012
82	eDP Mux	D2_SEAN	03/05/2012
83	eDP Muxed Graphics Support	D2_SEAN	03/05/2012
84	Thunderbolt Connector A	D2_KEPLER	01/13/2012
85	Thunderbolt Connector B	D2_KEPLER	01/13/2012
86	LCD Backlight Driver (LP8545)	D2_KEPLER	01/13/2012
87	PCH VCCIO (1.05V) POWER SUPPLY	D2_KEPLER	01/13/2012
88	Power Sequencing EG/PCH S0	D2_KEPLER	01/13/2012
89	CPU Constraints	D2_KEPLER	01/13/2012
90	Memory Constraints	D2_KEPLER	01/13/2012

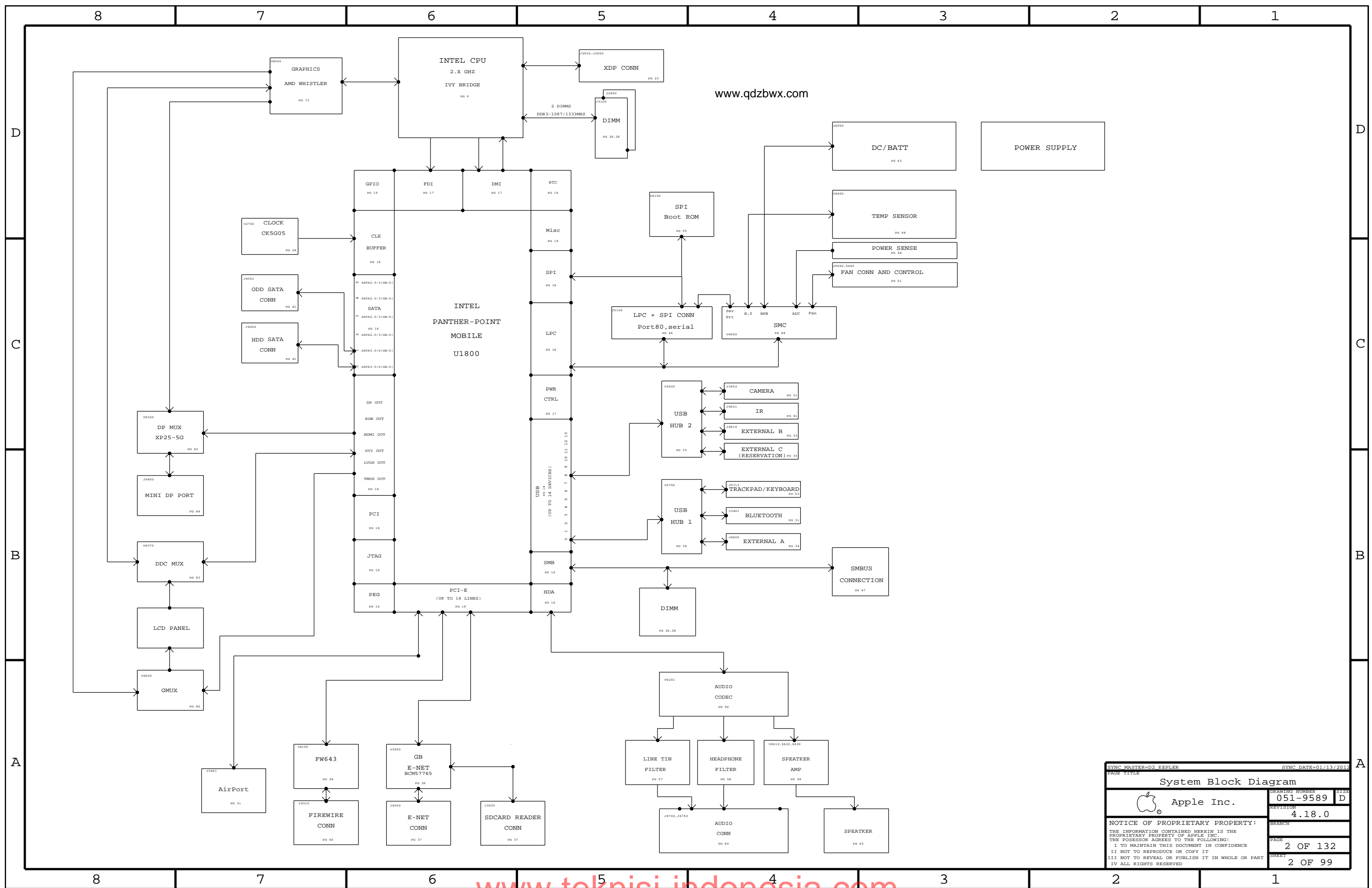
(.cma)		Date	
Page	Contents	Sync	
91	PCH Constraints 1	D2_KEPLER	01/13/2012
92	PCH Constraints 2	D2_KEPLER	01/13/2012
93	Thunderbolt Constraints	D2_KEPLER	01/13/2012
94	SMC Constraints	D2_KEPLER	01/13/2012
95	GPU (Kepler) CONSTRAINTS	D2_KEPLER	01/13/2012
96	Project Specific Constraints	D2_CLEAN	03/15/2012
97	PCB Rule Definitions	D2_KEPLER	01/13/2012
98	DEBUG SENSORS AND ADC	D2_SEAN	03/05/2012
99	SMC12 SENSORS EXTENDED	D2_KEPLER	01/13/2012


Schematic / PCB #'s

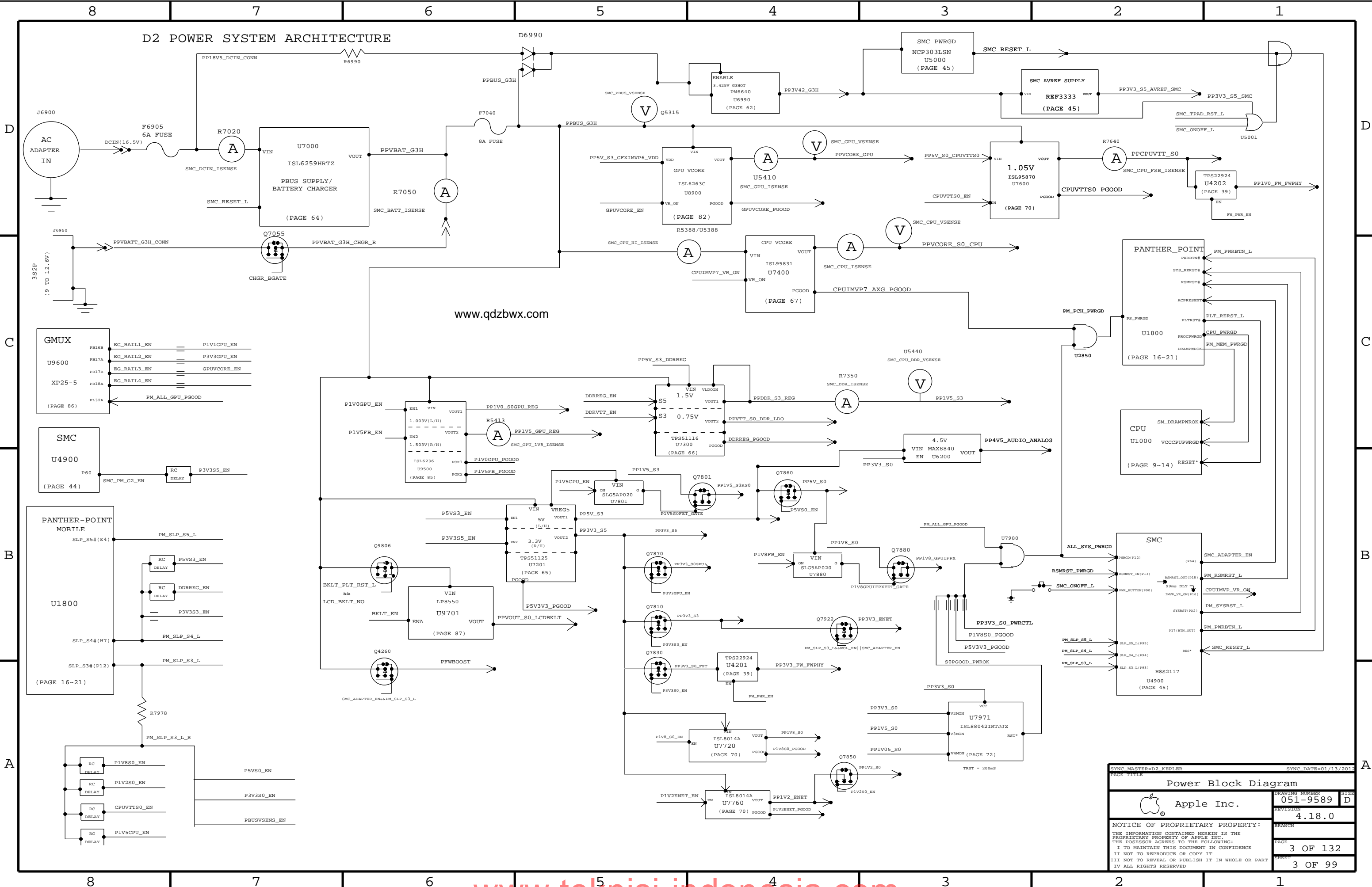
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9589	1	SCHEM,MLB,KEPLER_2PHASE,D2	SCH	CRITICAL	
820-3332	1	PCBF,MLB,KEPLER_2PHASE,D2	PCB	CRITICAL	


DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Wed May 9 13:50:52 2012

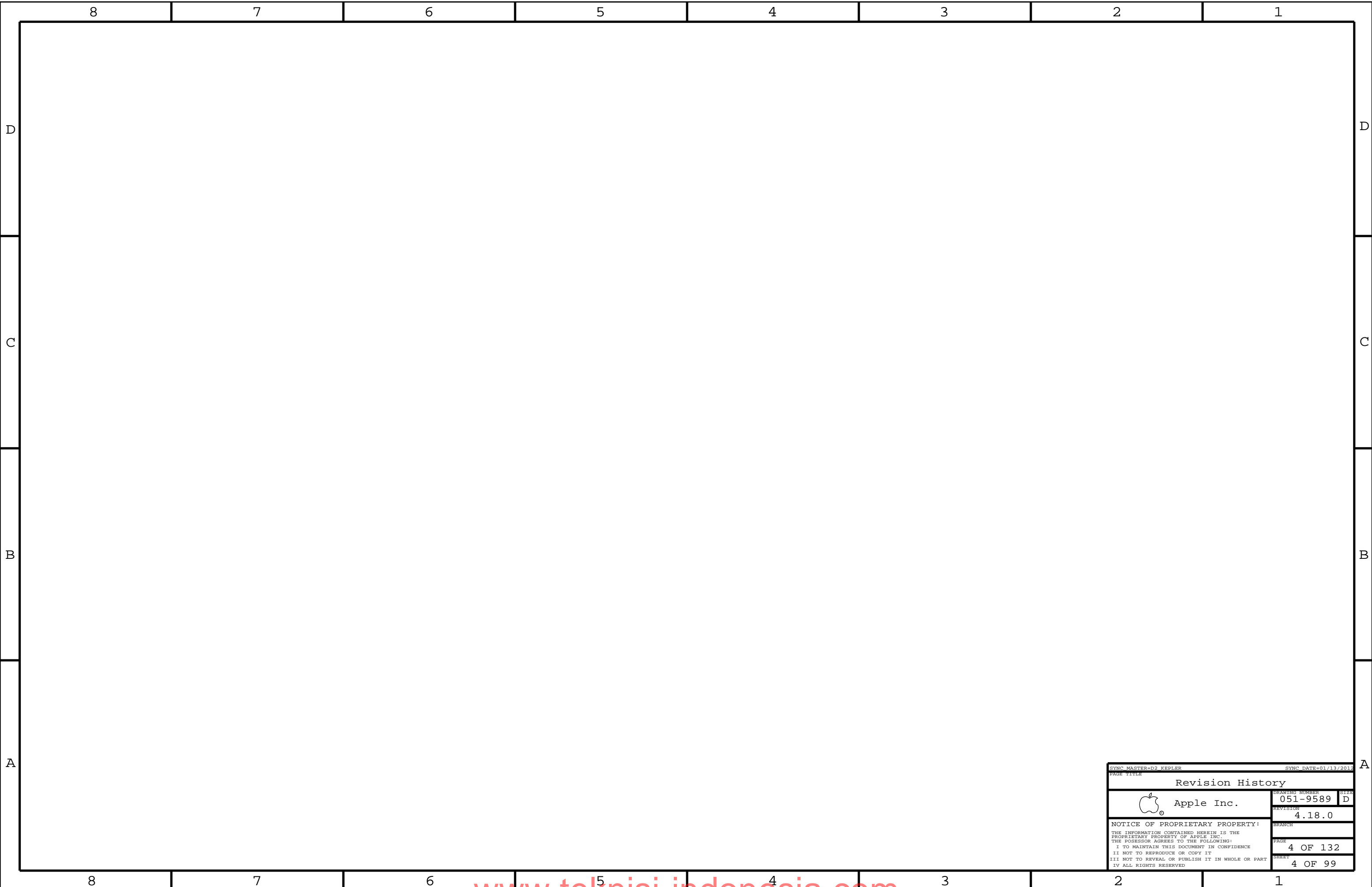
DRAWING TITLE		
SCHEM, MLB, KEPLER, 2PHASE, D2		
	Apple Inc.	
	DRAWING NUMBER 051-9589	
REVISION 4.18.0		SIZE D
NOTICE OF PROPRIETARY PROPERTY:		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		
BRANCH		PAGE 1 OF 132
SHEET		1 OF 99



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
System Block Diagram			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE D
	REVISION	4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		2 OF 132	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		2 OF 99	
IV ALL RIGHTS RESERVED			




SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
Power Block Diagram			
	Apple Inc.	DRAWING NUMBER	051-9589
		SIZE	D
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		PAGE 3 OF 132	
IV ALL RIGHTS RESERVED		SHEET 3 OF 99	



SYNC MASTER=D2 KEPPLER

SYNC DATE=01/13/2012

Revision History

 Apple Inc.

DRAWING NUMBER

051-9589

SIZE

D

REVISION

4.18.0

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE

4 OF 132

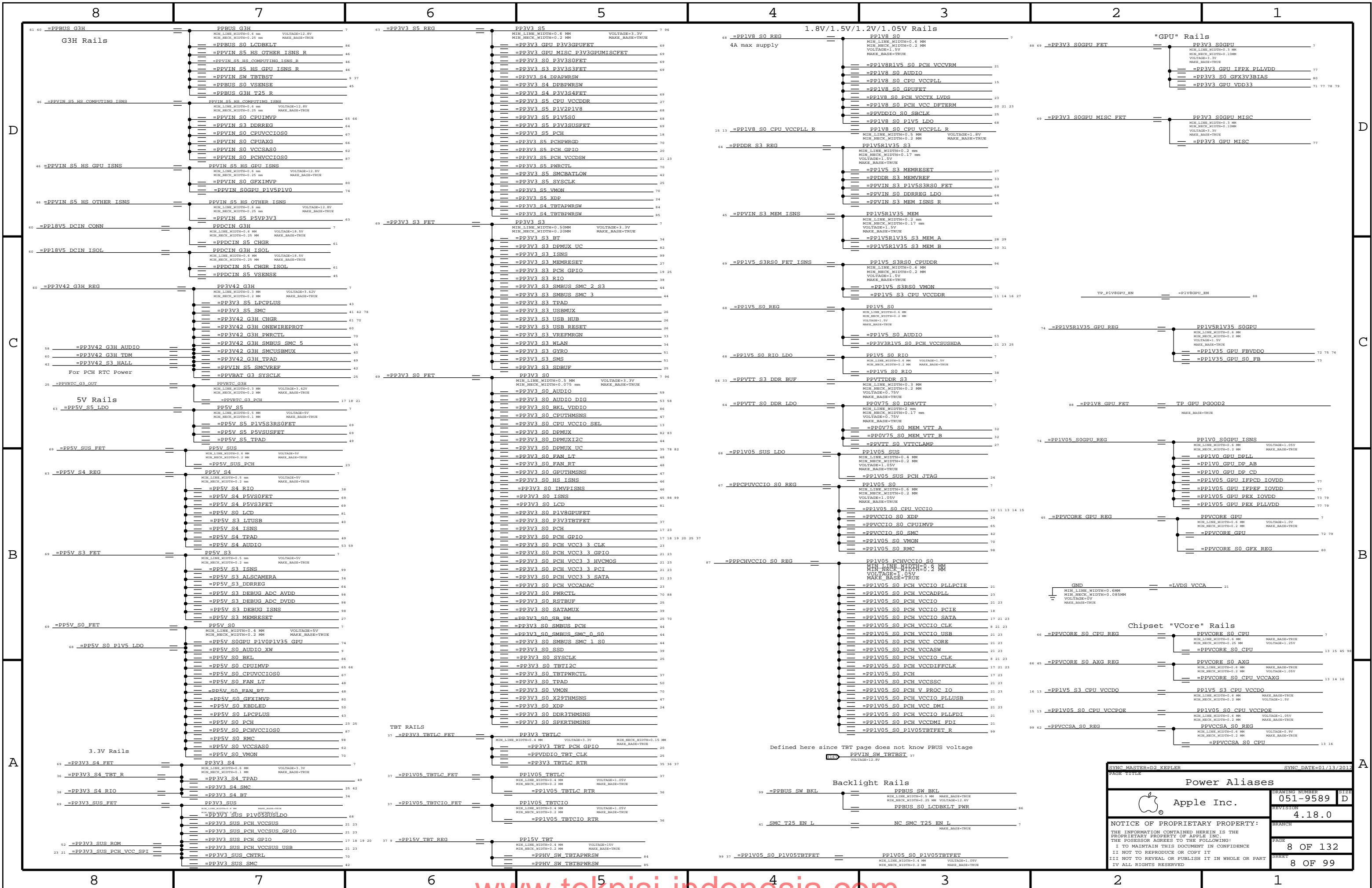
SHEET

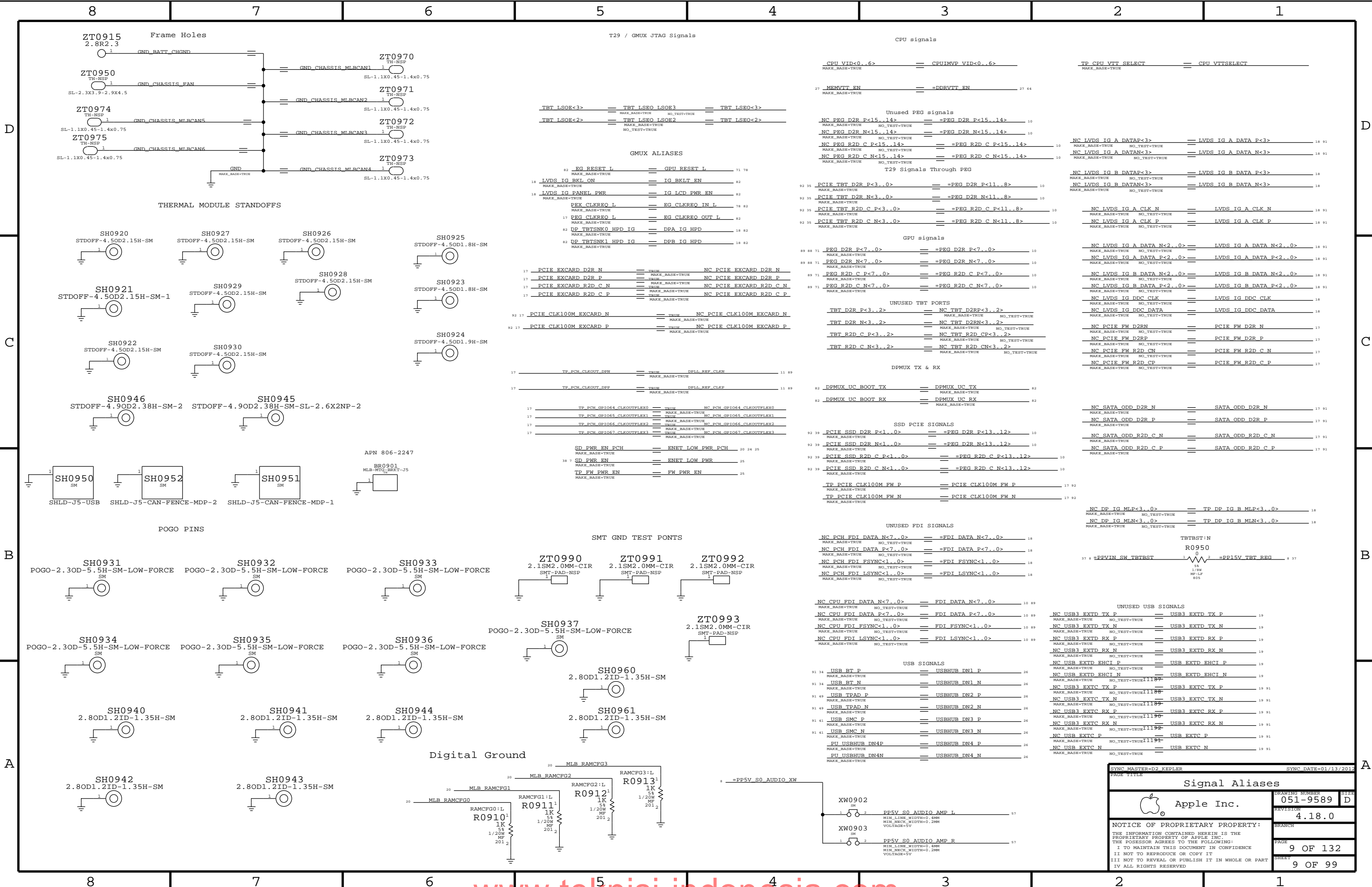
4 OF 99

www.teknisi-indonesia.com

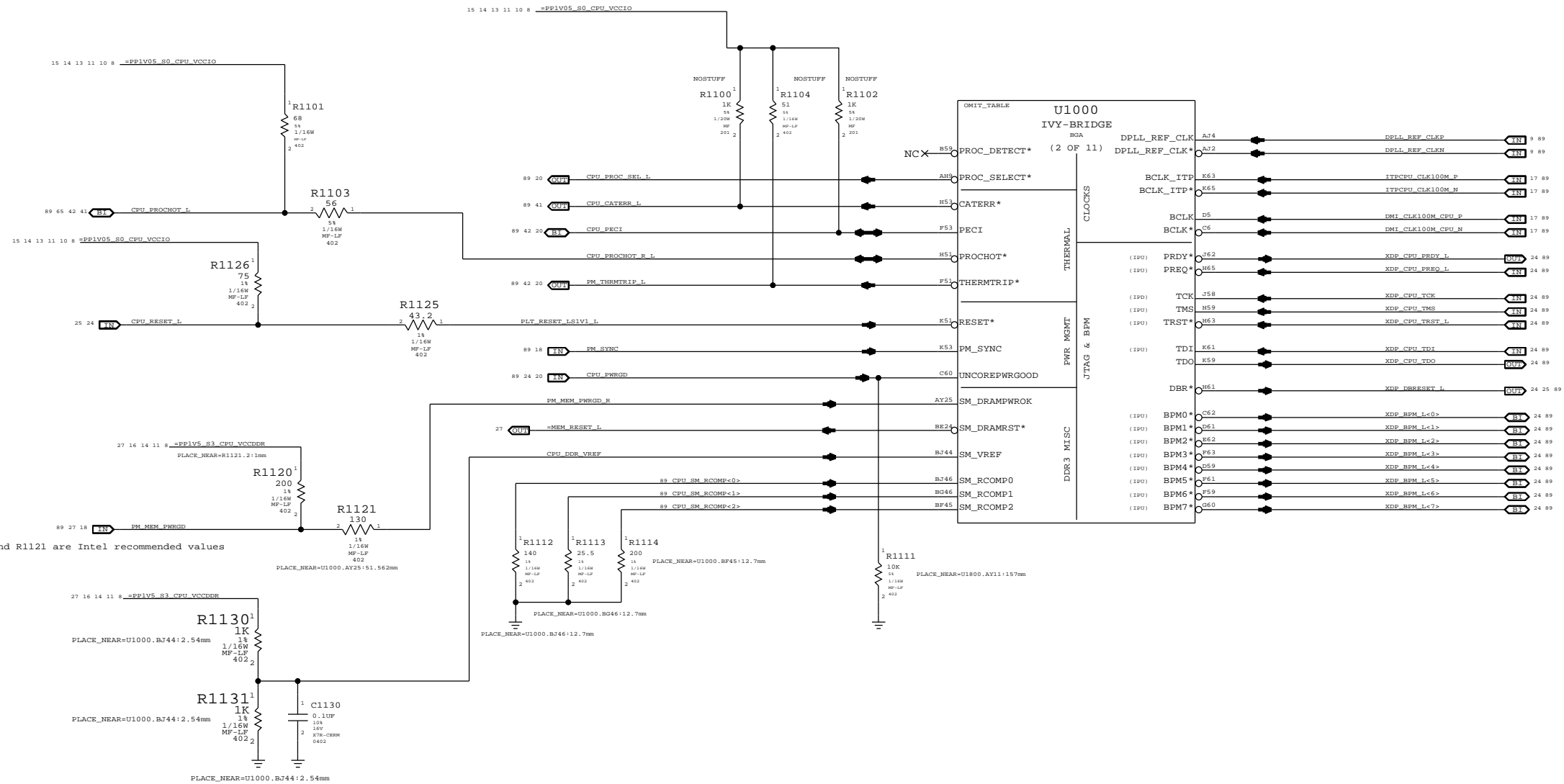
	8	7	6	5	4	3	2	1																																																																																																																																																													
	BOM Variants (continued on CSA 6)						Alternate Parts																																																																																																																																																														
	<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>085-3726</td><td>D2,MLB,KEPLER,DEV</td><td>D2_DEVEL:ENG</td></tr><tr><td>085-4776</td><td>D2,MLB,KEPLER,FSB DEV</td><td>D2_DEVEL:FSB</td></tr><tr><td>607-9546</td><td>D2,MLB,KEPLER_2PHASE,COMMON</td><td>D2_COMMON,POSCAP_MYLAR_PAIR</td></tr><tr><td>685-0016</td><td>PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2</td><td>PBUS_CAP:KEMET</td></tr><tr><td>685-0017</td><td>PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2</td><td>PBUS_CAP:SANYO</td></tr><tr><td>639-3378</td><td>PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3379</td><td>PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3380</td><td>PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3381</td><td>PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3384</td><td>PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3385</td><td>PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3386</td><td>PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-3387</td><td>PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C</td><td>BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-2821</td><td>PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-2825</td><td>PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-2817</td><td>PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-2815</td><td>PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-2979</td><td>PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-2980</td><td>PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-2981</td><td>PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-2982</td><td>PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G</td><td>BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-3618</td><td>PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3619</td><td>PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600</td></tr><tr><td>639-3561</td><td>PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3620</td><td>PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600</td></tr><tr><td>639-3627</td><td>PCBA,2.7G,16G_HYN,VRAIX_A_DIE,KEER:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3562</td><td>PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600</td></tr><tr><td>639-3628</td><td>PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr><tr><td>639-3629</td><td>PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT</td><td>BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600</td></tr></table>	BOM NUMBER	BOM NAME	BOM OPTIONS	085-3726	D2,MLB,KEPLER,DEV	D2_DEVEL:ENG	085-4776	D2,MLB,KEPLER,FSB DEV	D2_DEVEL:FSB	607-9546	D2,MLB,KEPLER_2PHASE,COMMON	D2_COMMON,POSCAP_MYLAR_PAIR	685-0016	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	PBUS_CAP:KEMET	685-0017	PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2	PBUS_CAP:SANYO	639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600	639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600	639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600	639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600	639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600	639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600	639-3627	PCBA,2.7G,16G_HYN,VRAIX_A_DIE,KEER:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600	639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600	639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600	Bar Code Labels / EEEE #'s (continued on CSA 6)																																																																									
BOM NUMBER	BOM NAME	BOM OPTIONS																																																																																																																																																																			
085-3726	D2,MLB,KEPLER,DEV	D2_DEVEL:ENG																																																																																																																																																																			
085-4776	D2,MLB,KEPLER,FSB DEV	D2_DEVEL:FSB																																																																																																																																																																			
607-9546	D2,MLB,KEPLER_2PHASE,COMMON	D2_COMMON,POSCAP_MYLAR_PAIR																																																																																																																																																																			
685-0016	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	PBUS_CAP:KEMET																																																																																																																																																																			
685-0017	PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2	PBUS_CAP:SANYO																																																																																																																																																																			
639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVV:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVV:2.6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600																																																																																																																																																																			
639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600																																																																																																																																																																			
639-3627	PCBA,2.7G,16G_HYN,VRAIX_A_DIE,KEER:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600																																																																																																																																																																			
639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVV:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600																																																																																																																																																																			
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY3V]</td><td>CRITICAL</td><td>EEEE:DY3V</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY3W]</td><td>CRITICAL</td><td>EEEE:DY3W</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY3Y]</td><td>CRITICAL</td><td>EEEE:DY3Y</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY40]</td><td>CRITICAL</td><td>EEEE:DY40</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY43]</td><td>CRITICAL</td><td>EEEE:DY43</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY44]</td><td>CRITICAL</td><td>EEEE:DY44</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY45]</td><td>CRITICAL</td><td>EEEE:DY45</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DY4C]</td><td>CRITICAL</td><td>EEEE:DY4C</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DRF1]</td><td>CRITICAL</td><td>EEEE:DRF1</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DRF4]</td><td>CRITICAL</td><td>EEEE:DRF4</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DRDN]</td><td>CRITICAL</td><td>EEEE:DRDN</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DRDW]</td><td>CRITICAL</td><td>EEEE:DRDW</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DT9H]</td><td>CRITICAL</td><td>EEEE:DT9H</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DT9D]</td><td>CRITICAL</td><td>EEEE:DT9D</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DT9F]</td><td>CRITICAL</td><td>EEEE:DT9F</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DT9G]</td><td>CRITICAL</td><td>EEEE:DT9G</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:F0HN]</td><td>CRITICAL</td><td>EEEE:F0HN</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:F0HR]</td><td>CRITICAL</td><td>EEEE:F0HR</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DWY4]</td><td>CRITICAL</td><td>EEEE:DWY4</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:F0HV]</td><td>CRITICAL</td><td>EEEE:F0HV</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:F0HM]</td><td>CRITICAL</td><td>EEEE:F0HM</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:DWY5]</td><td>CRITICAL</td><td>EEEE:DWY5</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:F0HY]</td><td>CRITICAL</td><td>EEEE:F0HY</td></tr><tr><td>825-7563</td><td>1</td><td>LABEL,MLB/L10,MBA</td><td>[EEEE:F0HT]</td><td>CRITICAL</td><td>EEEE:F0HT</td></tr></table>	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY3V]	CRITICAL	EEEE:DY3V	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY3W]	CRITICAL	EEEE:DY3W	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY3Y]	CRITICAL	EEEE:DY3Y	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY40]	CRITICAL	EEEE:DY40	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY43]	CRITICAL	EEEE:DY43	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY44]	CRITICAL	EEEE:DY44	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY45]	CRITICAL	EEEE:DY45	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY4C]	CRITICAL	EEEE:DY4C	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRF1]	CRITICAL	EEEE:DRF1	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRF4]	CRITICAL	EEEE:DRF4	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRDN]	CRITICAL	EEEE:DRDN	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRDW]	CRITICAL	EEEE:DRDW	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9H]	CRITICAL	EEEE:DT9H	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9D]	CRITICAL	EEEE:DT9D	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9F]	CRITICAL	EEEE:DT9F	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9G]	CRITICAL	EEEE:DT9G	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HN]	CRITICAL	EEEE:F0HN	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HR]	CRITICAL	EEEE:F0HR	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DWY4]	CRITICAL	EEEE:DWY4	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HV]	CRITICAL	EEEE:F0HV	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HM]	CRITICAL	EEEE:F0HM	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DWY5]	CRITICAL	EEEE:DWY5	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HY]	CRITICAL	EEEE:F0HY	825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HT]	CRITICAL	EEEE:F0HT	Programmables													
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY3V]	CRITICAL	EEEE:DY3V																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY3W]	CRITICAL	EEEE:DY3W																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY3Y]	CRITICAL	EEEE:DY3Y																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY40]	CRITICAL	EEEE:DY40																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY43]	CRITICAL	EEEE:DY43																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY44]	CRITICAL	EEEE:DY44																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY45]	CRITICAL	EEEE:DY45																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DY4C]	CRITICAL	EEEE:DY4C																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRF1]	CRITICAL	EEEE:DRF1																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRF4]	CRITICAL	EEEE:DRF4																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRDN]	CRITICAL	EEEE:DRDN																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DRDW]	CRITICAL	EEEE:DRDW																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9H]	CRITICAL	EEEE:DT9H																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9D]	CRITICAL	EEEE:DT9D																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9F]	CRITICAL	EEEE:DT9F																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DT9G]	CRITICAL	EEEE:DT9G																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HN]	CRITICAL	EEEE:F0HN																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HR]	CRITICAL	EEEE:F0HR																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DWY4]	CRITICAL	EEEE:DWY4																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HV]	CRITICAL	EEEE:F0HV																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HM]	CRITICAL	EEEE:F0HM																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:DWY5]	CRITICAL	EEEE:DWY5																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HY]	CRITICAL	EEEE:F0HY																																																																																																																																																																
825-7563	1	LABEL,MLB/L10,MBA	[EEEE:F0HT]	CRITICAL	EEEE:F0HT																																																																																																																																																																
	<table><tr><td>34183584</td><td>1</td><td>IC,TRAPRO/VRAM,OPTICAL,ONL,00</td><td>U5701</td><td>CRITICAL</td><td>TPAD_PROC:PROG</td></tr><tr><td>33782983</td><td>1</td><td>IC,T9_PROC,QFN,BLANK</td><td>U5701</td><td>CRITICAL</td><td>TPAD_PROC:BLANK</td></tr><tr><td>34183597</td><td>1</td><td>IC,KEPROM,CANTO,KIDDE 18-11,P8B,00</td><td>U3690</td><td>CRITICAL</td><td>TBTROM:PROG</td></tr><tr><td>3380865</td><td>1</td><td>KEPROM,CEARCT,QFN,1MM6,1,RY,2030W</td><td>U3690</td><td>CRITICAL</td><td>TBTROM:BLANK</td></tr><tr><td>3380852</td><td>1</td><td>IC,GPV,KOM,03,BLANK</td><td>U8701</td><td>CRITICAL</td><td>GPVROM:BLANK</td></tr><tr><td>34183565</td><td>1</td><td>IC,EEP,M8K-95C,(K8080A3) V1.2,8,009,00</td><td>U9100</td><td>CRITICAL</td><td>DPW0808C0:PROG</td></tr><tr><td>33784313</td><td>1</td><td>IC,M80,M80,1113,K8080,TSP-140V</td><td>U9100</td><td>CRITICAL</td><td>DPW0808C0:BLANK</td></tr></table>	34183584	1	IC,TRAPRO/VRAM,OPTICAL,ONL,00	U5701	CRITICAL	TPAD_PROC:PROG	33782983	1	IC,T9_PROC,QFN,BLANK	U5701	CRITICAL	TPAD_PROC:BLANK	34183597	1	IC,KEPROM,CANTO,KIDDE 18-11,P8B,00	U3690	CRITICAL	TBTROM:PROG	3380865	1	KEPROM,CEARCT,QFN,1MM6,1,RY,2030W	U3690	CRITICAL	TBTROM:BLANK	3380852	1	IC,GPV,KOM,03,BLANK	U8701	CRITICAL	GPVROM:BLANK	34183565	1	IC,EEP,M8K-95C,(K8080A3) V1.2,8,009,00	U9100	CRITICAL	DPW0808C0:PROG	33784313	1	IC,M80,M80,1113,K8080,TSP-140V	U9100	CRITICAL	DPW0808C0:BLANK	DRAM VREF Configs																																																																																																																									
34183584	1	IC,TRAPRO/VRAM,OPTICAL,ONL,00	U5701	CRITICAL	TPAD_PROC:PROG																																																																																																																																																																
33782983	1	IC,T9_PROC,QFN,BLANK	U5701	CRITICAL	TPAD_PROC:BLANK																																																																																																																																																																
34183597	1	IC,KEPROM,CANTO,KIDDE 18-11,P8B,00	U3690	CRITICAL	TBTROM:PROG																																																																																																																																																																
3380865	1	KEPROM,CEARCT,QFN,1MM6,1,RY,2030W	U3690	CRITICAL	TBTROM:BLANK																																																																																																																																																																
3380852	1	IC,GPV,KOM,03,BLANK	U8701	CRITICAL	GPVROM:BLANK																																																																																																																																																																
34183565	1	IC,EEP,M8K-95C,(K8080A3) V1.2,8,009,00	U9100	CRITICAL	DPW0808C0:PROG																																																																																																																																																																
33784313	1	IC,M80,M80,1113,K8080,TSP-140V	U9100	CRITICAL	DPW0808C0:BLANK																																																																																																																																																																
	<table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>VREF:PROD</td><td>VREFDQ:M1_M3,VREFCA:LDO</td></tr><tr><td>VREF:ENG_M3</td><td>VREFDQ:M1_M3,VREFCA:LDO_DAC</td></tr><tr><td>VREF:ENG_LDO</td><td>VREFDQ:M1_DAC,VREFCA:LDO_DAC</td></tr></table>	BOM GROUP	BOM OPTIONS	VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO	VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC	VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC	DRAM SPD Straps																																																																																																																																																											
BOM GROUP	BOM OPTIONS																																																																																																																																																																				
VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO																																																																																																																																																																				
VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC																																																																																																																																																																				
VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC																																																																																																																																																																				
	<table><tr><th>BOM GROUP</th><th>BOM OPTIONS</th></tr><tr><td>RAM_4G_HYNIX_1600_S</td><td>RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L</td></tr><tr><td>RAM_1G_SAMSUNG_1600</td><td>RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H</td></tr><tr><td>RAM_4G_SAMSUNG_1600_S</td><td>RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L</td></tr><tr><td>RAM_1G_HYNIX_1600</td><td>RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H</td></tr><tr><td>RAM_4G_ELPIDA_1600_S</td><td>RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L</td></tr><tr><td>RAM_2G_SAMSUNG_1600</td><td>2G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H</td></tr><tr><td>RAM_2G_SAMSUNG_1333</td><td>RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L</td></tr><tr><td>RAM_2G_HYNIX_1600</td><td>2G_HYNIX_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H</td></tr><tr><td>RAM_4G_SAMSUNG_1600</td><td>4G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L</td></tr><tr><td>RAM_4G_HYNIX_1600</td><td>4G_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H</td></tr><tr><td>RAM_2G_ELPIDA_1600_S</td><td>RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L</td></tr><tr><td>RAM_2G_ELPIDA_1600</td><td>2G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H</td></tr><tr><td>RAM_4G_ELPIDA_1600</td><td>4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L</td></tr><tr><td>RAM_2G_SAMSUNG_1600_S</td><td>RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H</td></tr><tr><td>RAM_2G_HYNIX_1600_S</td><td>RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L</td></tr></table>	BOM GROUP	BOM OPTIONS	RAM_4G_HYNIX_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L	RAM_1G_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H	RAM_4G_SAMSUNG_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L	RAM_1G_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H	RAM_4G_ELPIDA_1600_S	RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L	RAM_2G_SAMSUNG_1600	2G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H	RAM_2G_SAMSUNG_1333	RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L	RAM_2G_HYNIX_1600	2G_HYNIX_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H	RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L	RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H	RAM_2G_ELPIDA_1600_S	RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L	RAM_2G_ELPIDA_1600	2G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H	RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L	RAM_2G_SAMSUNG_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H	RAM_2G_HYNIX_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L	DEVELOPMENT/BASE BOM																																																																																																																																			
BOM GROUP	BOM OPTIONS																																																																																																																																																																				
RAM_4G_HYNIX_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L																																																																																																																																																																				
RAM_1G_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H																																																																																																																																																																				
RAM_4G_SAMSUNG_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L																																																																																																																																																																				
RAM_1G_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H																																																																																																																																																																				
RAM_4G_ELPIDA_1600_S	RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L																																																																																																																																																																				
RAM_2G_SAMSUNG_1600	2G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H																																																																																																																																																																				
RAM_2G_SAMSUNG_1333	RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L																																																																																																																																																																				
RAM_2G_HYNIX_1600	2G_HYNIX_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H																																																																																																																																																																				
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L																																																																																																																																																																				
RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H																																																																																																																																																																				
RAM_2G_ELPIDA_1600_S	RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L																																																																																																																																																																				
RAM_2G_ELPIDA_1600	2G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H																																																																																																																																																																				
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L																																																																																																																																																																				
RAM_2G_SAMSUNG_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H																																																																																																																																																																				
RAM_2G_HYNIX_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L																																																																																																																																																																				
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>085-3726</td><td>1</td><td>D2 MLB KEPLER DEVEL BOM</td><td>DEVEL</td><td>CRITICAL</td><td>DEVEL_BOM</td></tr><tr><td>085-4776</td><td>1</td><td>D2 MLB KEPLER FSB DEVEL BOM</td><td>DEVEL_FSB</td><td>CRITICAL</td><td>DEVEL_FSB_BOM</td></tr><tr><td>607-9546</td><td>1</td><td>D2 MLB KEPLER 2PHASE BASE BOM</td><td>BASE</td><td>CRITICAL</td><td>BASE_BOM</td></tr><tr><td>685-0016</td><td>1</td><td>PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2</td><td>POSCAP_MYLAR</td><td>CRITICAL</td><td>POSCAP_MYLAR_PAIR</td></tr></table>	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	085-3726	1	D2 MLB KEPLER DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM	085-4776	1	D2 MLB KEPLER FSB DEVEL BOM	DEVEL_FSB	CRITICAL	DEVEL_FSB_BOM	607-9546	1	D2 MLB KEPLER 2PHASE BASE BOM	BASE	CRITICAL	BASE_BOM	685-0016	1	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	POSCAP_MYLAR	CRITICAL	POSCAP_MYLAR_PAIR	SMC																																																																																																																																					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																																																																																
085-3726	1	D2 MLB KEPLER DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM																																																																																																																																																																
085-4776	1	D2 MLB KEPLER FSB DEVEL BOM	DEVEL_FSB	CRITICAL	DEVEL_FSB_BOM																																																																																																																																																																
607-9546	1	D2 MLB KEPLER 2PHASE BASE BOM	BASE	CRITICAL	BASE_BOM																																																																																																																																																																
685-0016	1	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	POSCAP_MYLAR	CRITICAL	POSCAP_MYLAR_PAIR																																																																																																																																																																
	<table><tr><td>34183308</td><td>1</td><td>IC,SMC,DEVELOPMENT-FSB,A3,00</td><td>U4900</td><td>CRITICAL</td><td>SMC_PROG:FSB</td></tr><tr><td>34183309</td><td>1</td><td>IC,SMC,PVB,A3,2,0PFA,00</td><td>U4900</td><td>CRITICAL</td><td>SMC_PROG:PVB</td></tr></table>	34183308	1	IC,SMC,DEVELOPMENT-FSB,A3,00	U4900	CRITICAL	SMC_PROG:FSB	34183309	1	IC,SMC,PVB,A3,2,0PFA,00	U4900	CRITICAL	SMC_PROG:PVB	EFI ROM																																																																																																																																																							
34183308	1	IC,SMC,DEVELOPMENT-FSB,A3,00	U4900	CRITICAL	SMC_PROG:FSB																																																																																																																																																																
34183309	1	IC,SMC,PVB,A3,2,0PFA,00	U4900	CRITICAL	SMC_PROG:PVB																																																																																																																																																																
	<table><tr><td>34183595</td><td>1</td><td>IC,EFI,ROM,FSB_00</td><td>U6100</td><td>CRITICAL</td><td>BOOTROM_PROG:FSB</td></tr></table>	34183595	1	IC,EFI,ROM,FSB_00	U6100	CRITICAL	BOOTROM_PROG:FSB																																																																																																																																																														
34183595	1	IC,EFI,ROM,FSB_00	U6100	CRITICAL	BOOTROM_PROG:FSB																																																																																																																																																																
	PD Parts																																																																																																																																																																				
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>33784266</td><td>1</td><td>IVB_8 ROM,P8Q,01,2.4,40K,4+2,1,2,0K,M0A</td><td>U1000</td><td>CRITICAL</td><td>CPU_IVV:2_SGE</td></tr><tr><td>33784267</td><td>1</td><td>IVB_8 ROM,P8Q,01,2.4,40K,4+2,1,25,0K,M0A</td><td>U1000</td><td>CRITICAL</td><td>CPU_IVV:2_SGEH</td></tr><tr><td>33784268</td><td>1</td><td>IVB_8 ROM,P8Q,01,2.7,40K,4+2,1,25,0K,M0A</td><td>U1000</td><td>CRITICAL</td><td>CPU_IVV:2_7GHE</td></tr><tr><td>33784269</td><td>1</td><td>PANTHER,PODCT,C1,0L29C,P8Q,00030077</td><td>U1800</td><td>CRITICAL</td><td></td></tr><tr><td>33784256</td><td>1</td><td>IC,GPV,MV,08107-078-F0-A3</td><td>U8000</td><td>CRITICAL</td><td></td></tr><tr><td>33881113</td><td>1</td><td>IC,TRF,TR,40,80,P8Q,C03,038 12012 P8Q-00P</td><td>U3600</td><td>CRITICAL</td><td>TBTROM:PROG</td></tr><tr><td>33380622</td><td>32</td><td>IC,080AM,0083-1600,250009,78P80A,001X,C-018,180M</td><td></td><td>CRITICAL</td><td>2G_HYNIX_1600</td></tr><tr><td>33380623</td><td>32</td><td>IC,080AM,0083-1600,250009,78P80A,000100</td><td></td><td>CRITICAL</td><td>2G_SAMSUNG_1600</td></tr><tr><td>33380628</td><td>32</td><td>IC,080AM,0083-1600,250009,78P80A,0-018,ELPIDA</td><td></td><td>CRITICAL</td><td>2G_ELPIDA_1600</td></tr><tr><td>33380625</td><td>32</td><td>IC,080AM,0083-1600,512009,78P80A,001X</td><td></td><td>CRITICAL</td><td>4G_HYNIX_1600</td></tr><tr><td>33380624</td><td>32</td><td>IC,080AM,0083-1600,512009,78P80A,C-018,SAM080</td><td></td><td>CRITICAL</td><td>4G_SAMSUNG_1600</td></tr><tr><td>33380629</td><td>32</td><td>IC,080AM,0083-1600,512009,78P80A,0-018,ELPIDA</td><td></td><td>CRITICAL</td><td>4G_ELPIDA_1600</td></tr><tr><td>33380630</td><td>4</td><td>IC,080AM,00085,64M012,A-018,HYNIX</td><td>U8400,U8450,U8500,U8550</td><td>CRITICAL</td><td>FB_2G_HYNIX_A_DIE</td></tr><tr><td>33380631</td><td>4</td><td>IC,080AM,00085,64M012,B-018,SAM080</td><td>U8400,U8450,U8500,U8550</td><td>CRITICAL</td><td>FB_2G_SAMSUNG</td></tr><tr><td>12850264</td><td>30</td><td>CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E</td><td></td><td>CRITICAL</td><td>PBUS_CAP:SANYO</td></tr><tr><td>12850257</td><td>30</td><td>CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF</td><td></td><td>CRITICAL</td><td>PBUS_CAP:KEMET</td></tr><tr><td>725-1614</td><td>1</td><td>INSULATOR,SHORT,REAR,MLB,D2</td><td>REAR_INSULATOR</td><td>CRITICAL</td><td>PBUS_CAP:SANYO</td></tr><tr><td>725-1648</td><td>1</td><td>INSULATOR,TALL,REAR,MLB,D2</td><td>REAR_INSULATOR</td><td>CRITICAL</td><td>PBUS_CAP:KEMET</td></tr><tr><td>725-1568</td><td>1</td><td>INSULATOR,CPU,D2</td><td>CPU_INSULATOR</td><td>CRITICAL</td><td></td></tr><tr><td>725-1569</td><td>1</td><td>INSULATOR,GPU,D2</td><td>GPU_INSULATOR</td><td>CRITICAL</td><td></td></tr><tr><td>725-1621</td><td>1</td><td>INSULATOR,PCH,D2</td><td>PCH_INSULATOR</td><td>CRITICAL</td><td></td></tr><tr><td>806-2897</td><td>2</td><td>CAN,COVER,2,J5</td><td>CAN_COVER1,CAN_COVER2</td><td>CRITICAL</td><td></td></tr><tr><td>825-7697</td><td>1</td><td>TEXT,LABEL,MLB,D2</td><td>TEXT_LABEL</td><td>CRITICAL</td><td></td></tr><tr><td>946-3819</td><td>1</td><td>D2 MLB DYNAX ADHESIVE SRE-CURE 29993-SC</td><td>EDGE_BOND</td><td>CRITICAL</td><td></td></tr><tr><td>825-7841</td><td>1</td><td>LBL,PART CONFIG,BOARDS,D2</td><td>CONFIG_LABEL</td><td>CRITICAL</td><td></td></tr></table>	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	33784266	1	IVB_8 ROM,P8Q,01,2.4,40K,4+2,1,2,0K,M0A	U1000	CRITICAL	CPU_IVV:2_SGE	33784267	1	IVB_8 ROM,P8Q,01,2.4,40K,4+2,1,25,0K,M0A	U1000	CRITICAL	CPU_IVV:2_SGEH	33784268	1	IVB_8 ROM,P8Q,01,2.7,40K,4+2,1,25,0K,M0A	U1000	CRITICAL	CPU_IVV:2_7GHE	33784269	1	PANTHER,PODCT,C1,0L29C,P8Q,00030077	U1800	CRITICAL		33784256	1	IC,GPV,MV,08107-078-F0-A3	U8000	CRITICAL		33881113	1	IC,TRF,TR,40,80,P8Q,C03,038 12012 P8Q-00P	U3600	CRITICAL	TBTROM:PROG	33380622	32	IC,080AM,0083-1600,250009,78P80A,001X,C-018,180M		CRITICAL	2G_HYNIX_1600	33380623	32	IC,080AM,0083-1600,250009,78P80A,000100		CRITICAL	2G_SAMSUNG_1600	33380628	32	IC,080AM,0083-1600,250009,78P80A,0-018,ELPIDA		CRITICAL	2G_ELPIDA_1600	33380625	32	IC,080AM,0083-1600,512009,78P80A,001X		CRITICAL	4G_HYNIX_1600	33380624	32	IC,080AM,0083-1600,512009,78P80A,C-018,SAM080		CRITICAL	4G_SAMSUNG_1600	33380629	32	IC,080AM,0083-1600,512009,78P80A,0-018,ELPIDA		CRITICAL	4G_ELPIDA_1600	33380630	4	IC,080AM,00085,64M012,A-018,HYNIX	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_HYNIX_A_DIE	33380631	4	IC,080AM,00085,64M012,B-018,SAM080	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_SAMSUNG	12850264	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E		CRITICAL	PBUS_CAP:SANYO	12850257	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF		CRITICAL	PBUS_CAP:KEMET	725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO	725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET	725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL		725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL		725-1621	1	INSULATOR,PCH,D2	PCH_INSULATOR	CRITICAL		806-2897	2	CAN,COVER,2,J5	CAN_COVER1,CAN_COVER2	CRITICAL		825-7697	1	TEXT,LABEL,MLB,D2	TEXT_LABEL	CRITICAL		946-3819	1	D2 MLB DYNAX ADHESIVE SRE-CURE 29993-SC	EDGE_BOND	CRITICAL		825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL									
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																																																																																																																
33784266	1	IVB_8 ROM,P8Q,01,2.4,40K,4+2,1,2,0K,M0A	U1000	CRITICAL	CPU_IVV:2_SGE																																																																																																																																																																
33784267	1	IVB_8 ROM,P8Q,01,2.4,40K,4+2,1,25,0K,M0A	U1000	CRITICAL	CPU_IVV:2_SGEH																																																																																																																																																																
33784268	1	IVB_8 ROM,P8Q,01,2.7,40K,4+2,1,25,0K,M0A	U1000	CRITICAL	CPU_IVV:2_7GHE																																																																																																																																																																
33784269	1	PANTHER,PODCT,C1,0L29C,P8Q,00030077	U1800	CRITICAL																																																																																																																																																																	
33784256	1	IC,GPV,MV,08107-078-F0-A3	U8000	CRITICAL																																																																																																																																																																	
33881113	1	IC,TRF,TR,40,80,P8Q,C03,038 12012 P8Q-00P	U3600	CRITICAL	TBTROM:PROG																																																																																																																																																																
33380622	32	IC,080AM,0083-1600,250009,78P80A,001X,C-018,180M		CRITICAL	2G_HYNIX_1600																																																																																																																																																																
33380623	32	IC,080AM,0083-1600,250009,78P80A,000100		CRITICAL	2G_SAMSUNG_1600																																																																																																																																																																
33380628	32	IC,080AM,0083-1600,250009,78P80A,0-018,ELPIDA		CRITICAL	2G_ELPIDA_1600																																																																																																																																																																
33380625	32	IC,080AM,0083-1600,512009,78P80A,001X		CRITICAL	4G_HYNIX_1600																																																																																																																																																																
33380624	32	IC,080AM,0083-1600,512009,78P80A,C-018,SAM080		CRITICAL	4G_SAMSUNG_1600																																																																																																																																																																
33380629	32	IC,080AM,0083-1600,512009,78P80A,0-018,ELPIDA		CRITICAL	4G_ELPIDA_1600																																																																																																																																																																
33380630	4	IC,080AM,00085,64M012,A-018,HYNIX	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_HYNIX_A_DIE																																																																																																																																																																
33380631	4	IC,080AM,00085,64M012,B-018,SAM080	U8400,U8450,U8500,U8550	CRITICAL	FB_2G_SAMSUNG																																																																																																																																																																
12850264	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E		CRITICAL	PBUS_CAP:SANYO																																																																																																																																																																
12850257	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF		CRITICAL	PBUS_CAP:KEMET																																																																																																																																																																
725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO																																																																																																																																																																
725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET																																																																																																																																																																
725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL																																																																																																																																																																	
725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL																																																																																																																																																																	
725-1621	1	INSULATOR,PCH,D2	PCH_INSULATOR	CRITICAL																																																																																																																																																																	
806-2897	2	CAN,COVER,2,J5	CAN_COVER1,CAN_COVER2	CRITICAL																																																																																																																																																																	
825-7697	1	TEXT,LABEL,MLB,D2	TEXT_LABEL	CRITICAL																																																																																																																																																																	
946-3819	1	D2 MLB DYNAX ADHESIVE SRE-CURE 29993-SC	EDGE_BOND	CRITICAL																																																																																																																																																																	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL																																																																																																																																																																	
	8	7	6	5	4	3	2	1																																																																																																																																																													

8	7	6	5	4	3	2	1	
BOM Variants (continued from CSA 5)			Bar Code Labels / EEEE #'s (continued from CSA 5)					
BOM NUMBER	BOM NAME	BOM OPTIONS	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
639-3382	PCBA, 2. 3G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, DY41	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY41,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY41]	CRITICAL	EEEE:DY41
639-3383	PCBA, 2. 3G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, DY42	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_SAMSUNG,EEEE:DY42,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY42]	CRITICAL	EEEE:DY42
639-3445	PCBA, 2. 3G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, DYJ5	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYJ5,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ5]	CRITICAL	EEEE:DYJ5
639-3446	PCBA, 2. 3G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, DYJ6	BASE_BOM,CPU_IVY:2.3GHZ,FB_2G_SAMSUNG,EEEE:DYJ6,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ6]	CRITICAL	EEEE:DYJ6
639-2818	PCBA, 2. 6G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, DRF0	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF0,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF0]	CRITICAL	EEEE:DRF0
639-2820	PCBA, 2. 6G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, DRDP	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDP,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDP]	CRITICAL	EEEE:DRDP
639-2823	PCBA, 2. 6G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, DRDT	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDT,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDT]	CRITICAL	EEEE:DRDT
639-2819	PCBA, 2. 6G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, DRDQ	BASE_BOM,CPU_IVY:2.6GHZ,FB_2G_SAMSUNG,EEEE:DRDQ,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDQ]	CRITICAL	EEEE:DRDQ
639-3632	PCBA, 2. 7G, 8G_ELP, VRAM_HYN, MLB_KEPLER, D2, F0JD	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0JD,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JD]	CRITICAL	EEEE:F0JD
639-3633	PCBA, 2. 7G, 8G_ELP, VRAM_SAM, MLB_KEPLER, D2, F0J3	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0J3,DEVEL_BOM,RAM_2G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J3]	CRITICAL	EEEE:F0J3
639-3630	PCBA, 2. 7G, 16G_ELP, VRAM_HYN, MLB_KEPLER, D2, F0J4	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0J4,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J4]	CRITICAL	EEEE:F0J4
639-3631	PCBA, 2. 7G, 16G_ELP, VRAM_SAM, MLB_KEPLER, D2, F0JC	BASE_BOM,CPU_IVY:2.7GHZ,FB_2G_SAMSUNG,EEEE:F0JC,DEVEL_BOM,RAM_4G_ELPIDA_1600	825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JC]	CRITICAL	EEEE:F0JC
			Elipda DQ'd Keeping for PRQ					





Signal Aliases		Drawing Number	051-9589	Size	D
Apple Inc.		Revision	4.18.0	Branch	
NOTICE OF PROPRIETARY PROPERTY:		Page	9 OF 132	Sheet	9 OF 99
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:					
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE					
II NOT TO REPRODUCE OR COPY IT					
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART					
IV ALL RIGHTS RESERVED					



R1120 and R1121 are Intel recommended values

PLACE_NEAR=U1000.AY25:51.562mm

PLACE_NEAR=U1000.BJ44:2.54mm

PLACE_NEAR=U1000.BJ44:2.54mm


PLACE_NEAR=U1000.BJ44:2.54mm

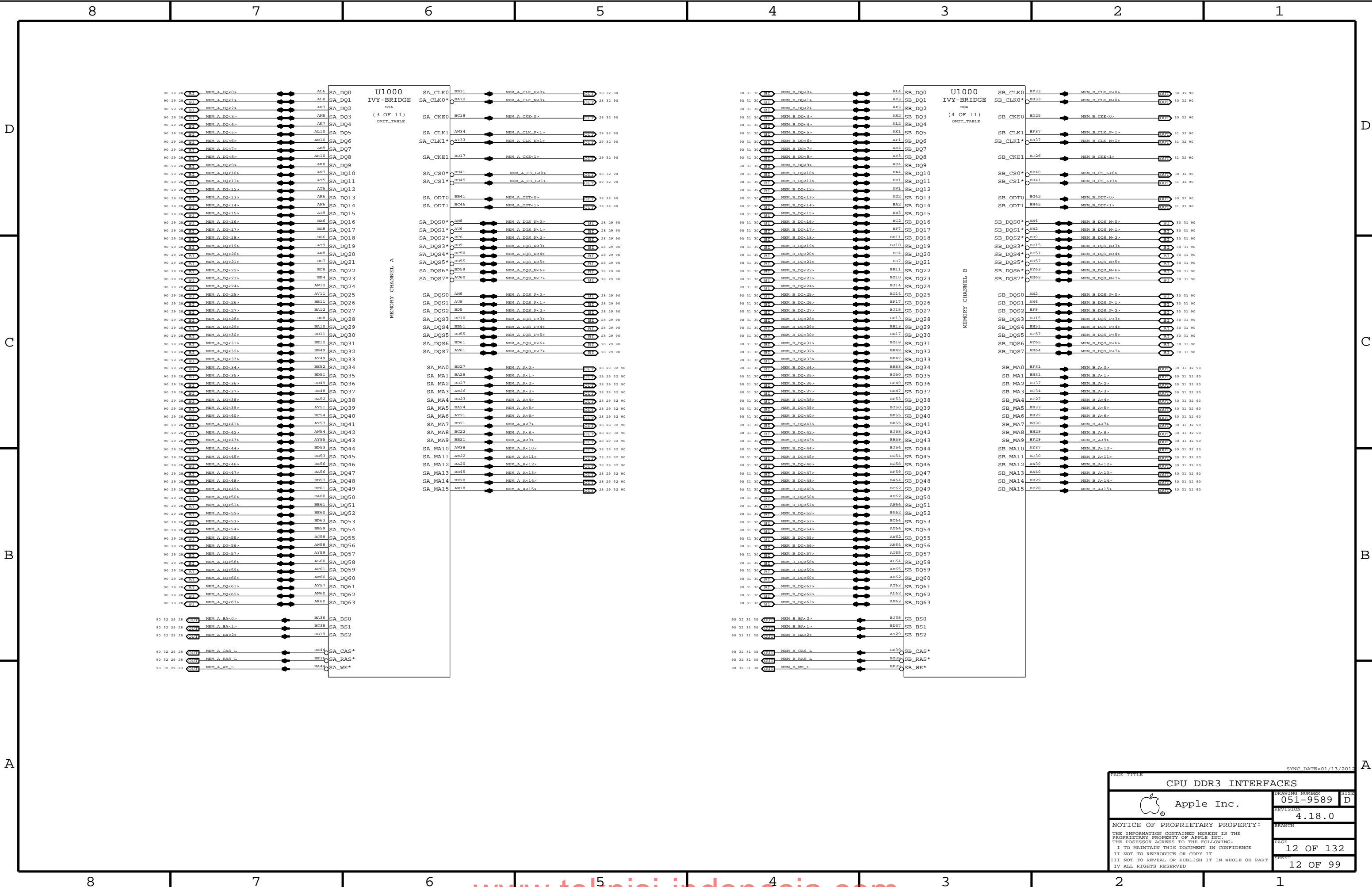
PLACE_NEAR=U1000.BJ46:12.7mm

PLACE_NEAR=U1000.BF45:12.7mm

PLACE_NEAR=U1000.BJ46:12.7mm

PLACE_NEAR=U1800.AY11:157mm

PAGE TITLE			
CPU CLOCK/MISC/JTAG			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE
	REVISION	4.18.0	D
	BRANCH		
	PAGE	11 OF 132	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
SHEET 11 OF 99			



D

C

B

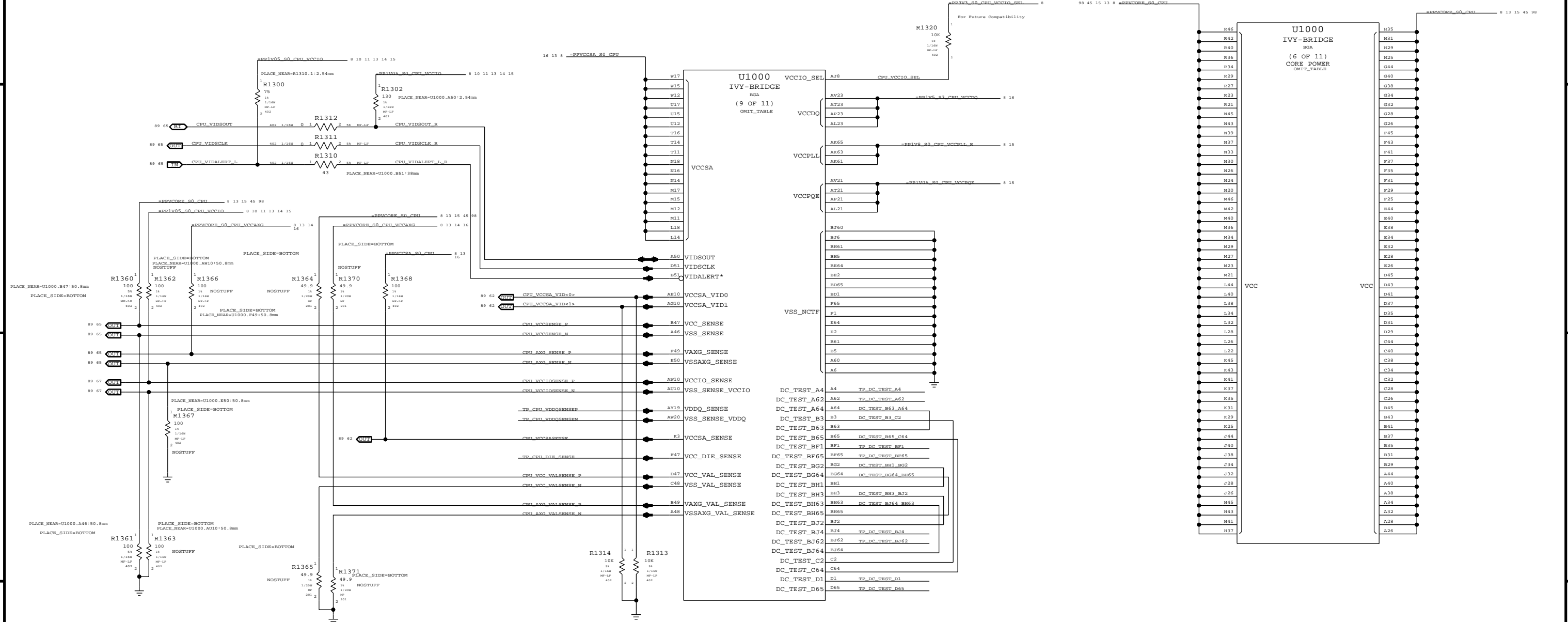
A


D

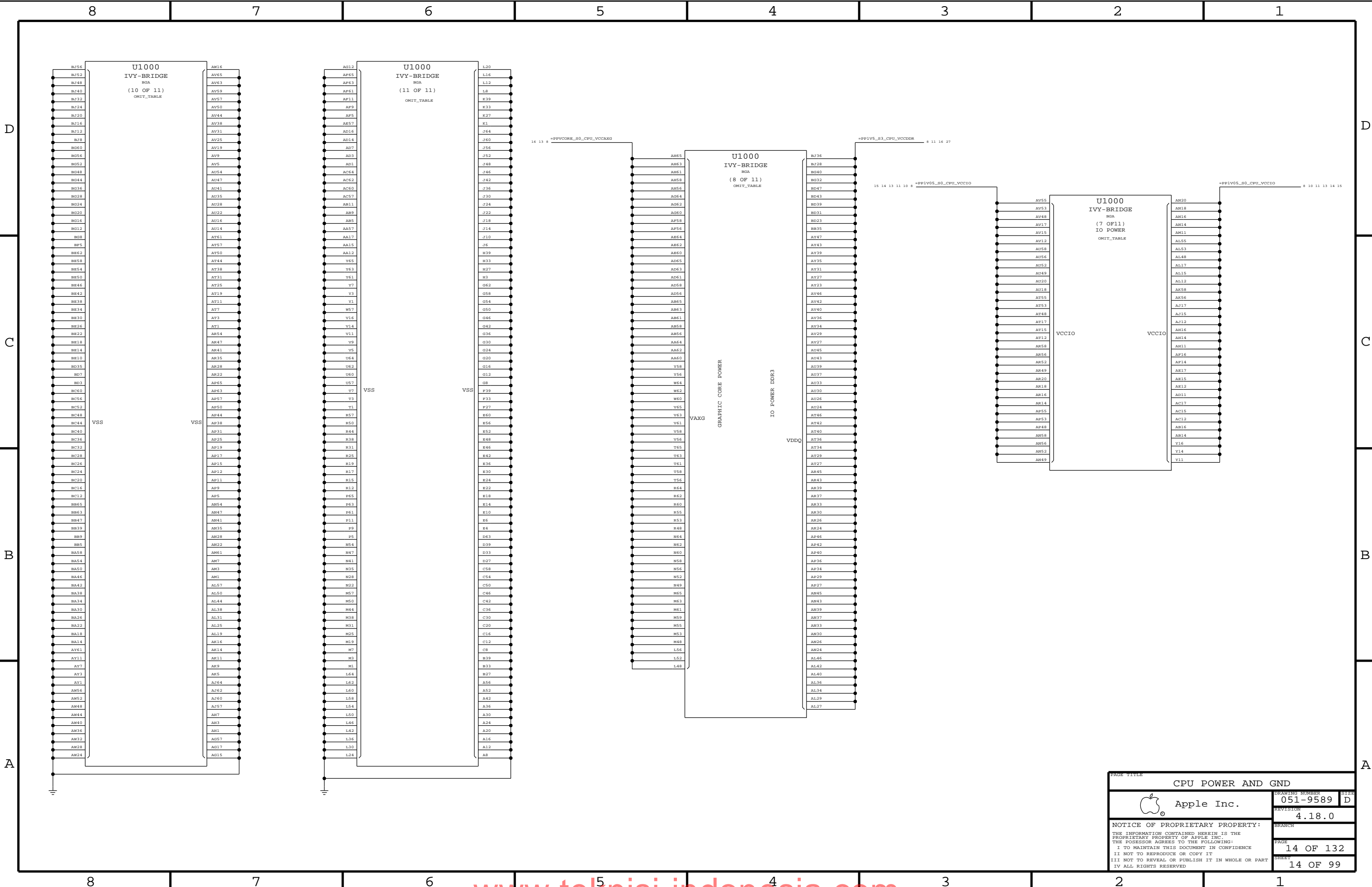
C

B

A



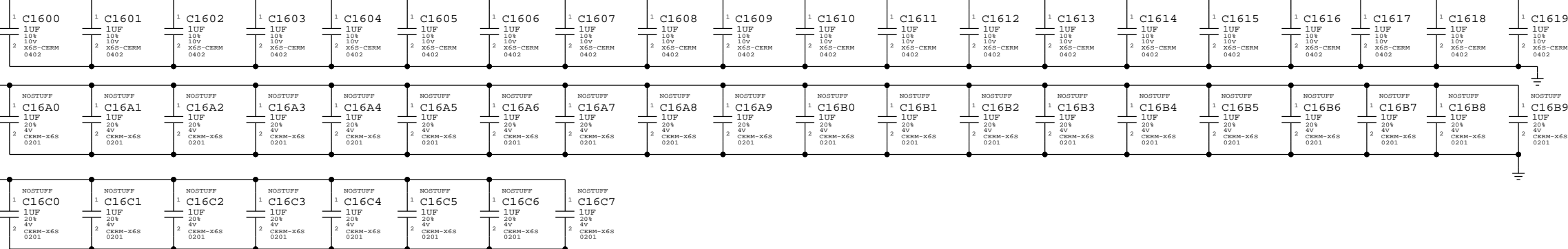
SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
CPU POWER			
 Apple Inc.	DRAWING NUMBER		SHEET
	051-9589		D
	REVISION		
4.18.0			
NOTICE OF PROPRIETARY PROPERTY:			
BRANCH			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
PAGE		13 OF 132	
SHEET		13 OF 99	



Apple Implementation: 8x 270uF 6mOhm, 0x 470uF 4mOhm, 16x 22uF 0402, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0402 (NOSTUFF)

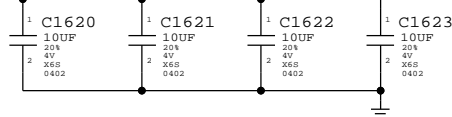
PLACEMENT_NOTE (C1600-C16C7):

Place on bottom side of U1000



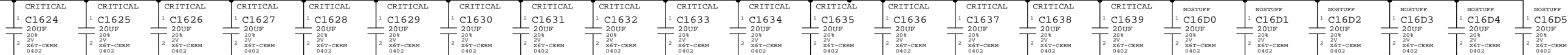
PLACEMENT_NOTE (C1620-C1623)

Place near inductors on bottom side.
Place near U1000 on bottom side

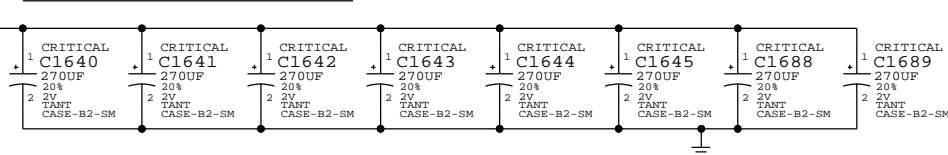


PLACEMENT_NOTE (C1624-C16D5)

Place near inductors on bottom side.



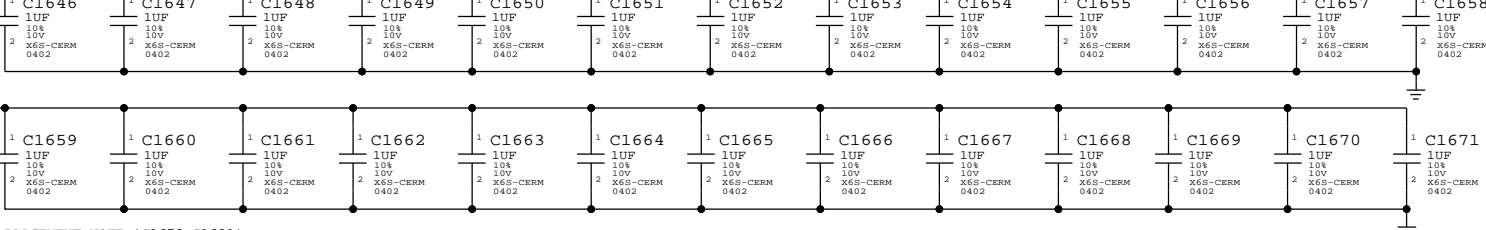
PLACEMENT_NOTE (C1640-C1645



```
Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
```

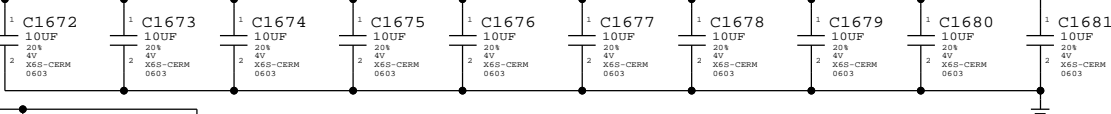
PLACEMENT_NOTE (C1646-C1671):

Place on bottom side of U1000



PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side



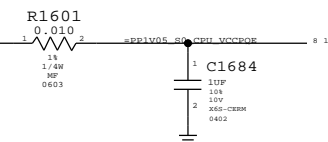
CRITICAL

1 C1682
330UF-6MOHM
20%
POLY-TANT
DIST-ECGLT-COMBO

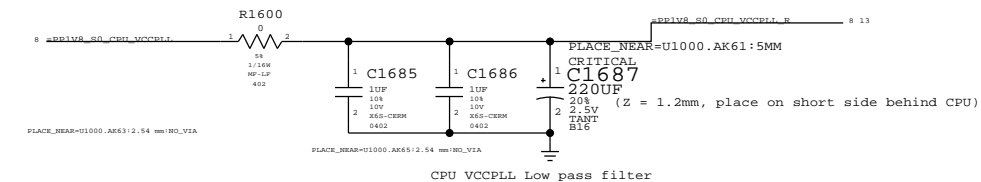
CRITICAL

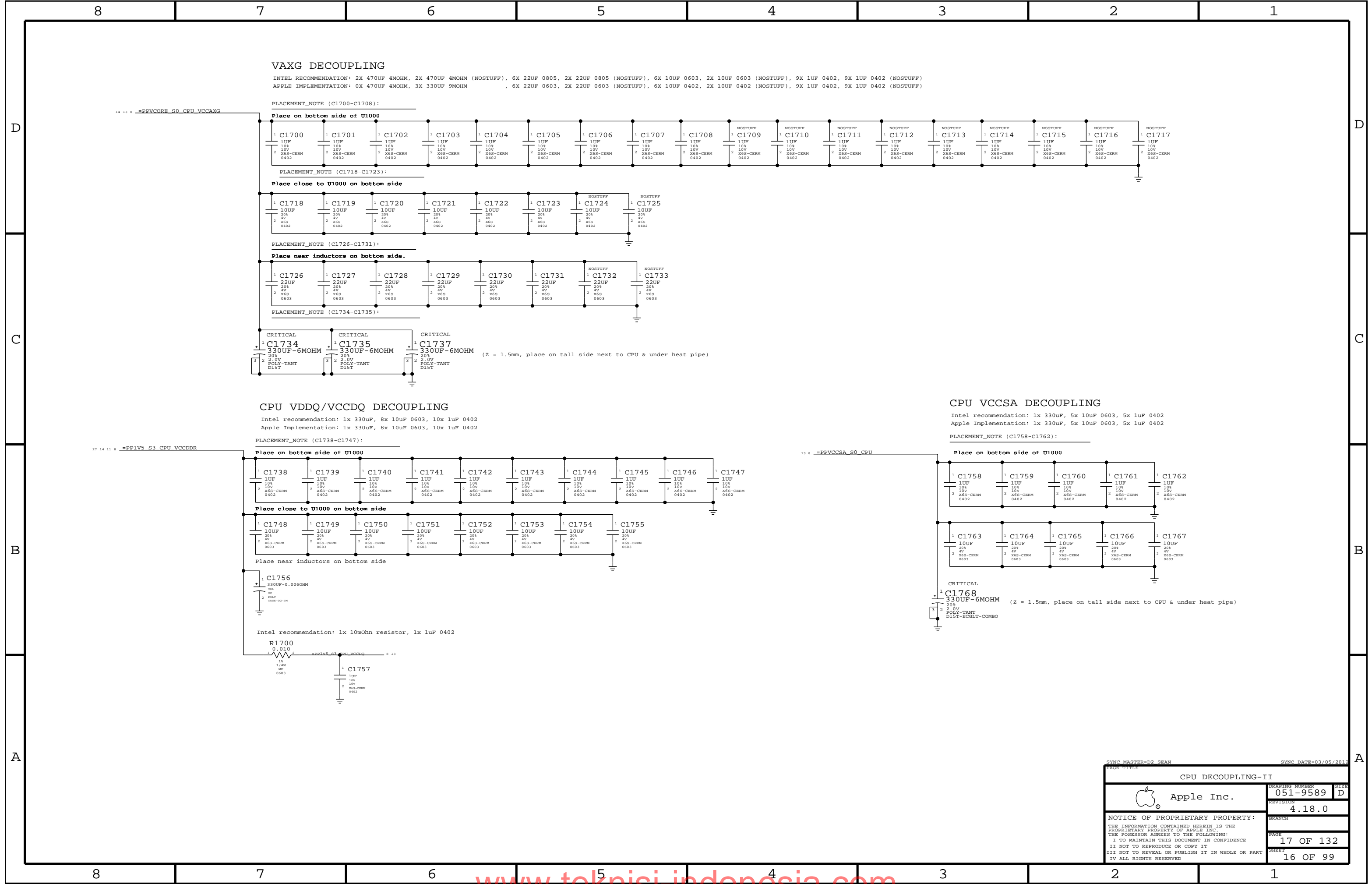
1 C1683
330UF-6MOHM
20%
POLY-TANT
DIST-ECGLT-COMBO

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



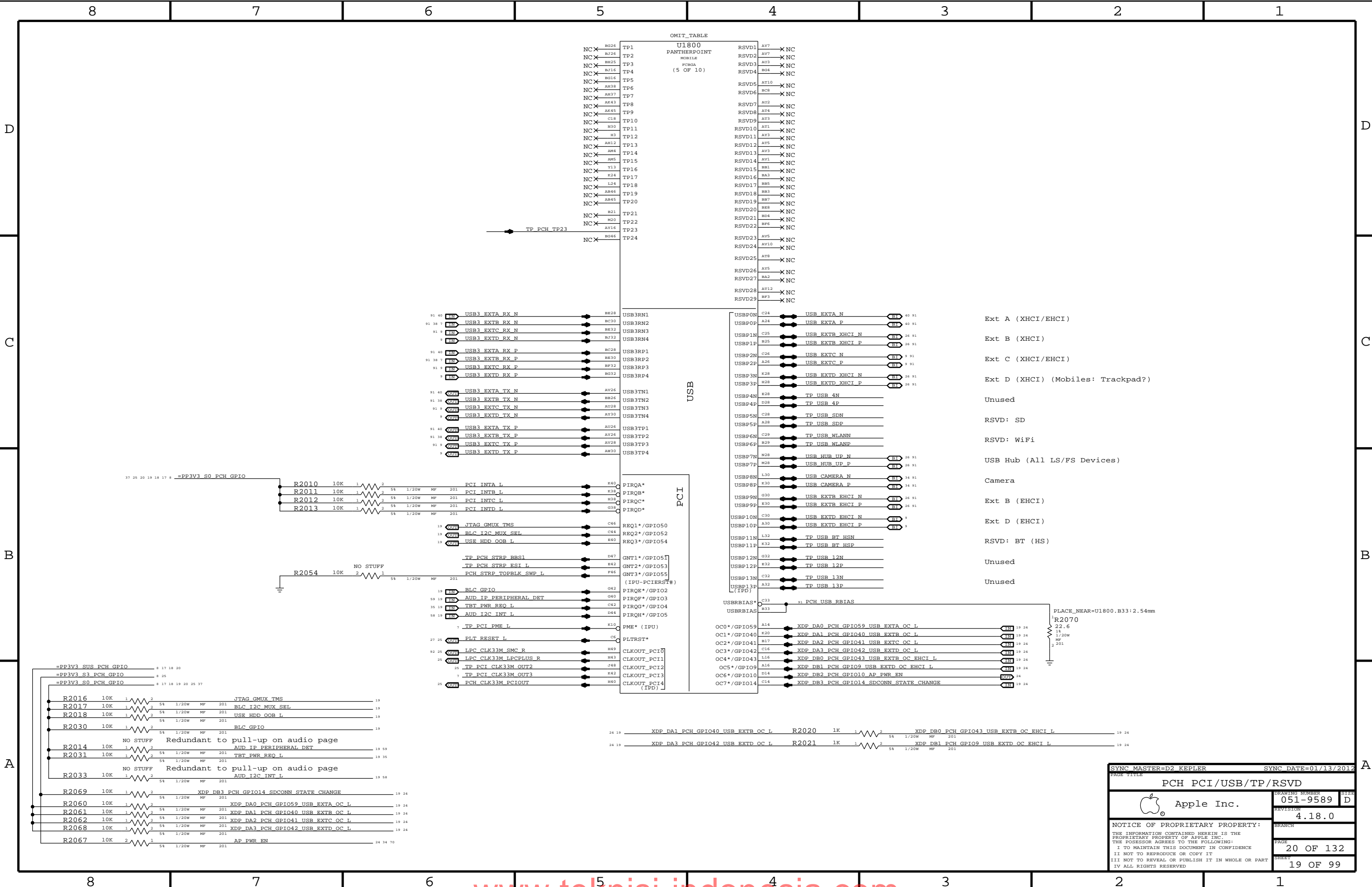
CPU VCCPLL DECOUPLING











Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

051-9589

4.18.0

20 OF 132

19 OF 99

20 OF 132

19 OF 99

20 OF 132

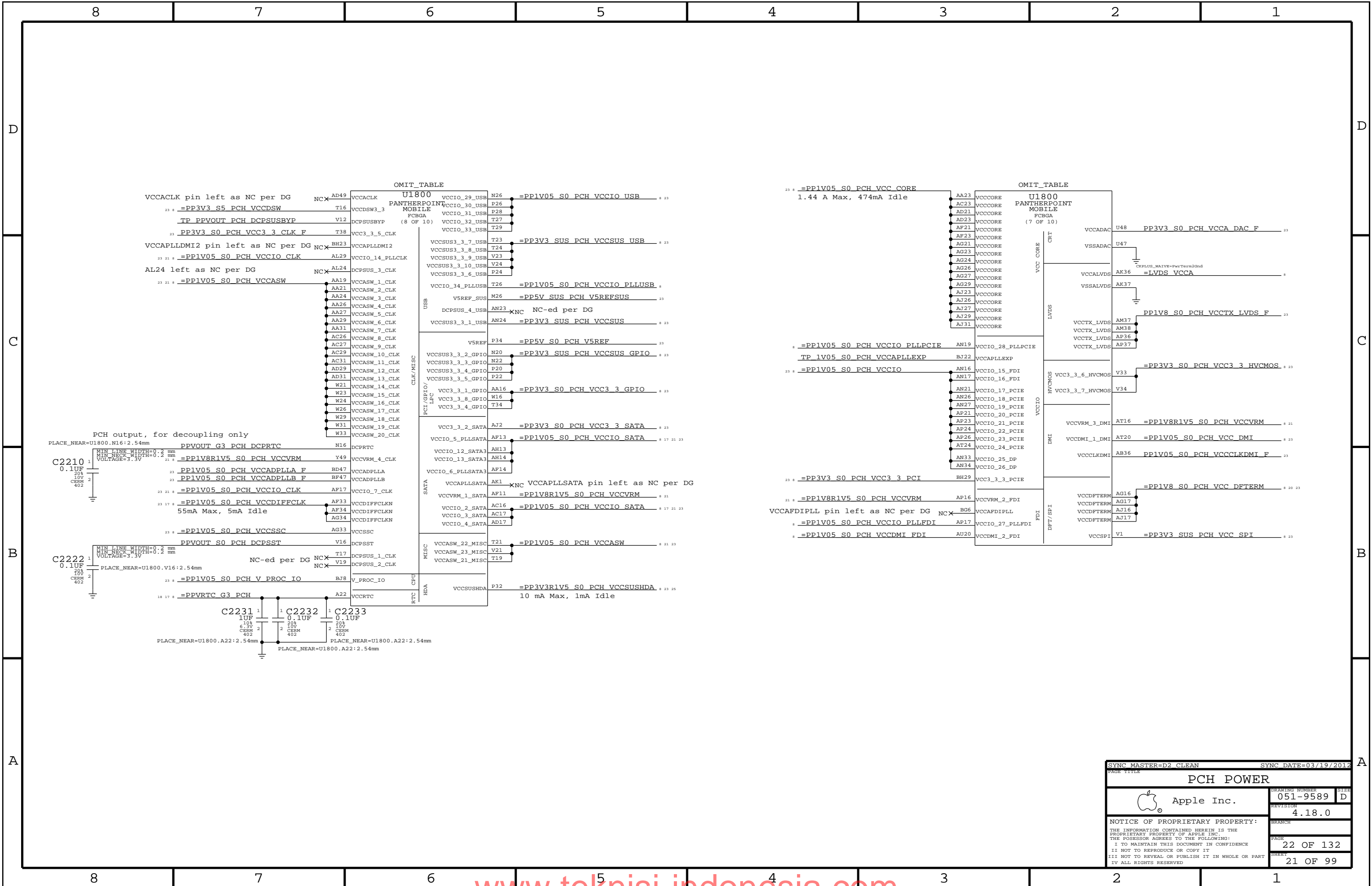
19 OF 99

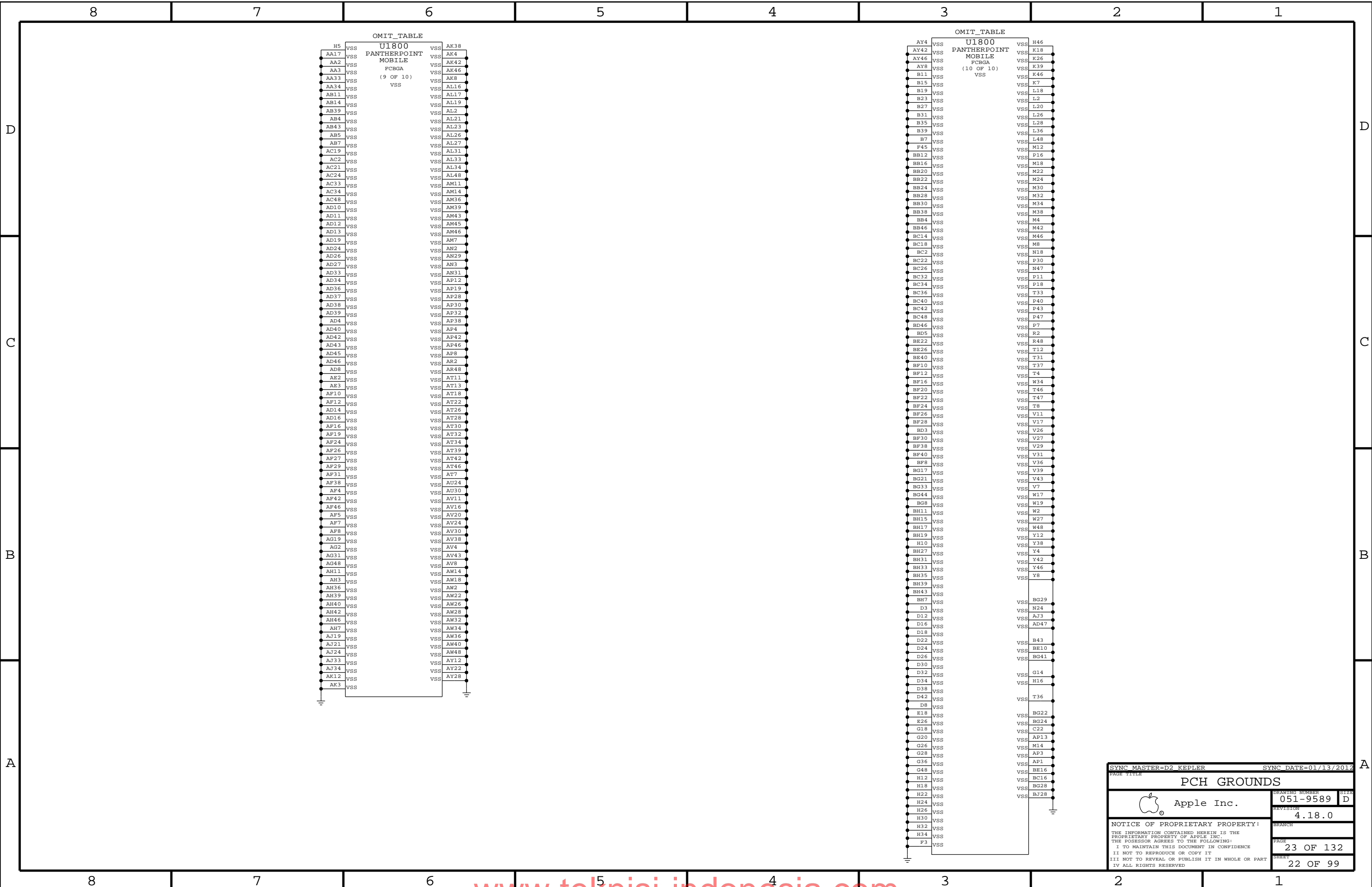
20 OF 132

19 OF 99

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012








SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

PAGE TITLE

PCH GROUNDS

 Apple Inc.

DRAWING NUMBER
051-9589

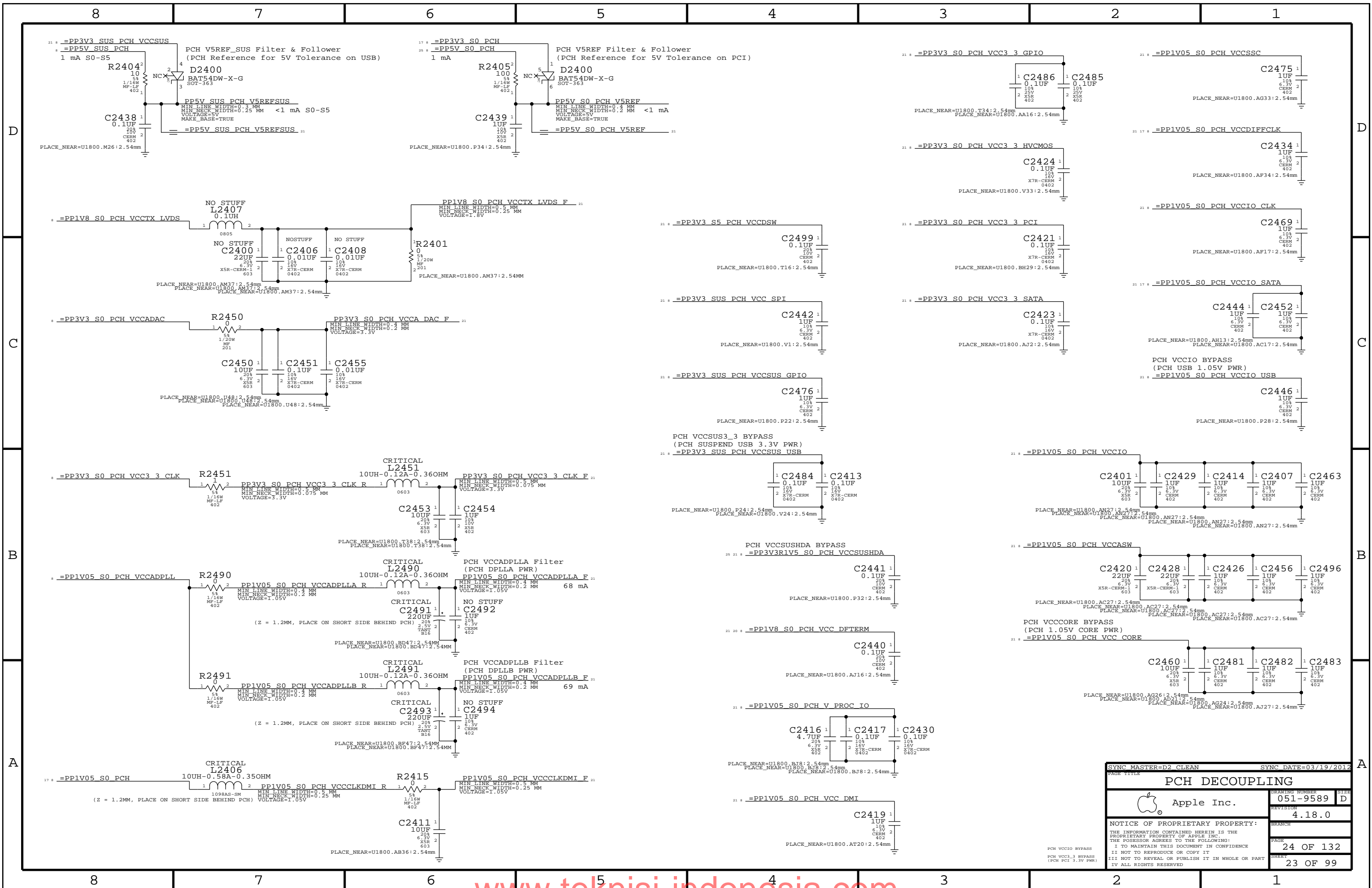
REVISION
4.18.0


BRANCH

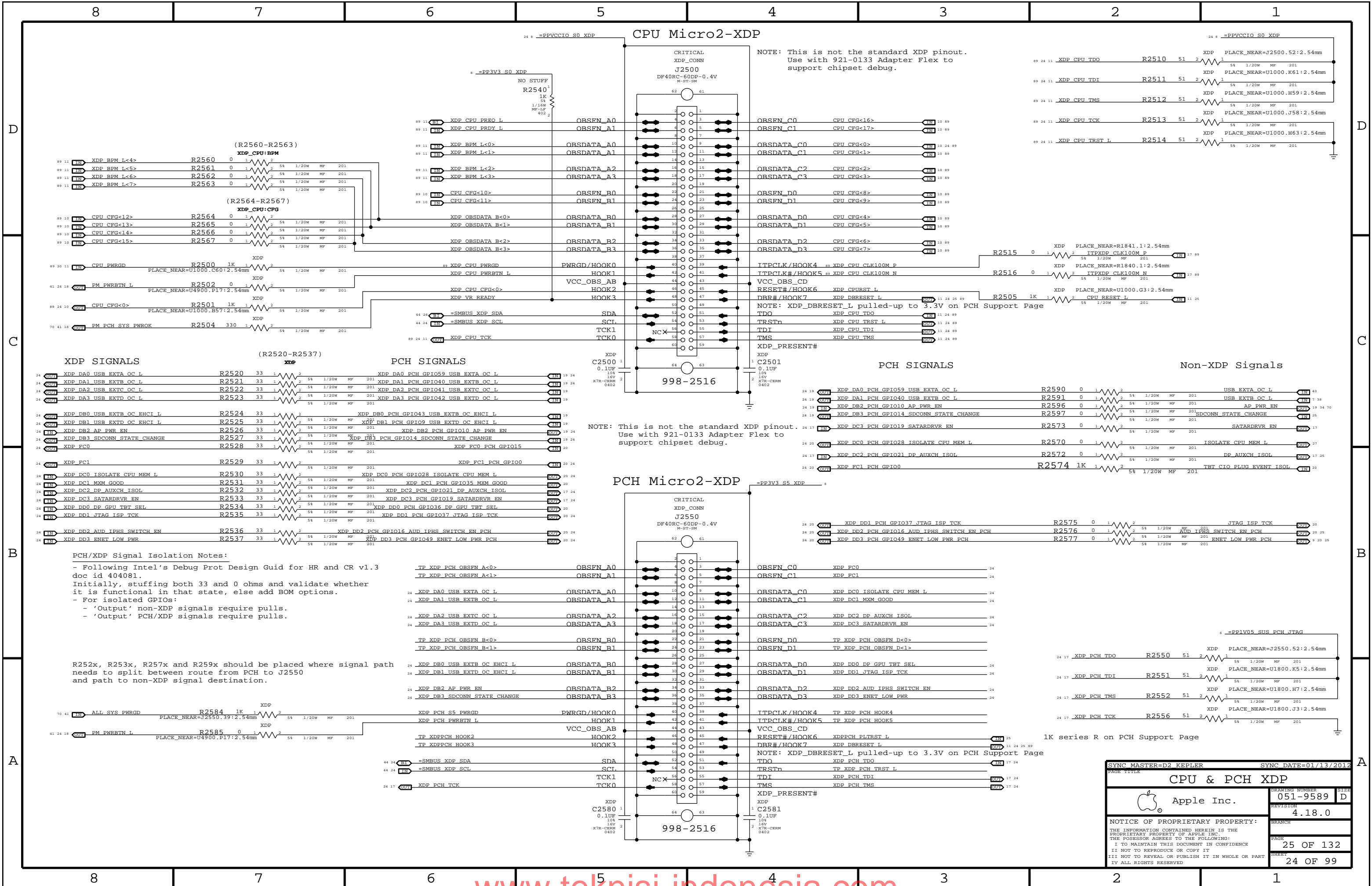
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE
23 OF 132

SHEET
22 OF 99



SYNC MASTER=D2 CLEAN		SYNC DATE=03/19/2012	
PAGE TITLE			
PCH DECOUPLING			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE
	REVISION	4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	24 OF 132
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	23 OF 99
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



D

C

D

C

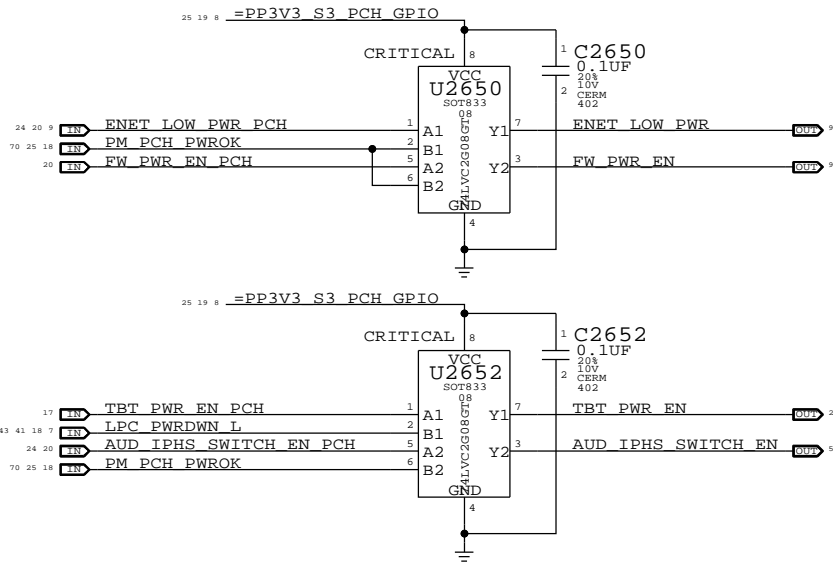
B

B

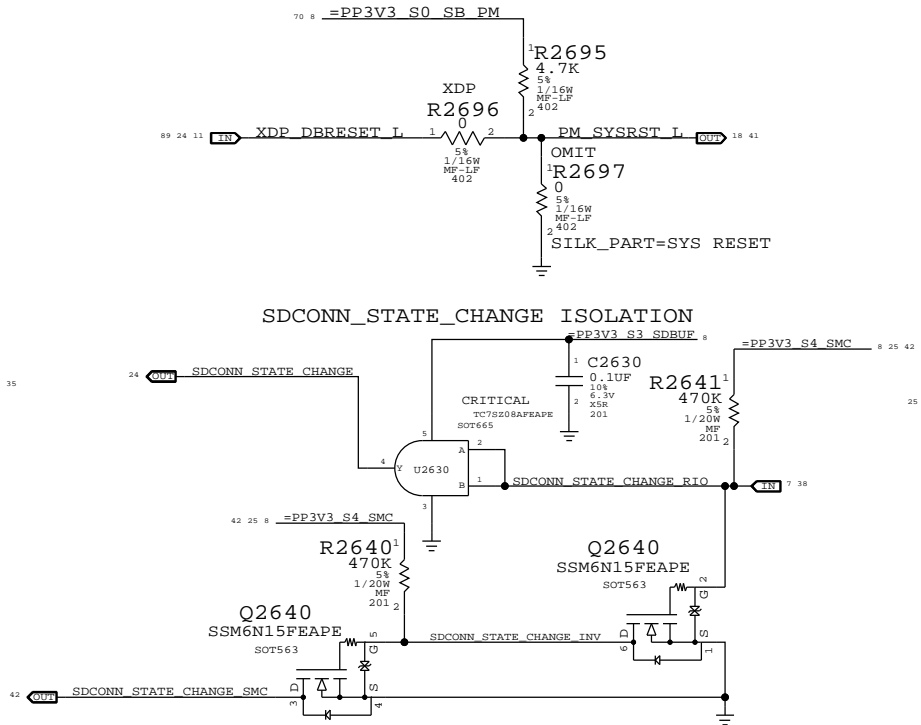
A

A

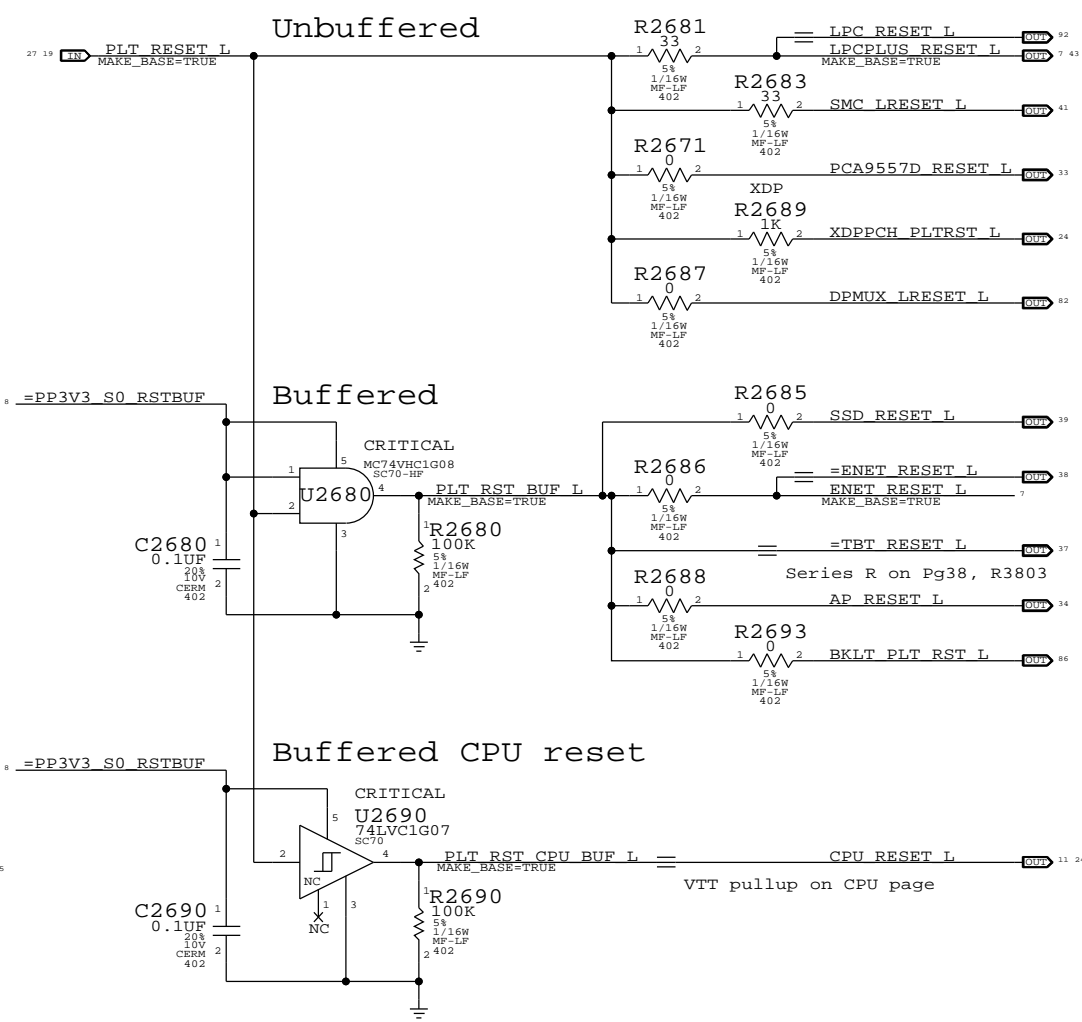
GPIO Glitch Prevention



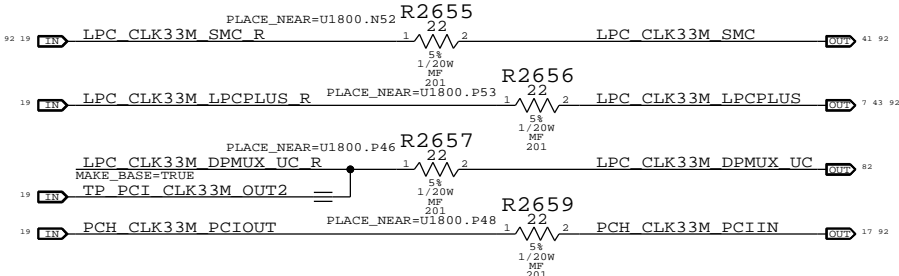
PCH Reset Button



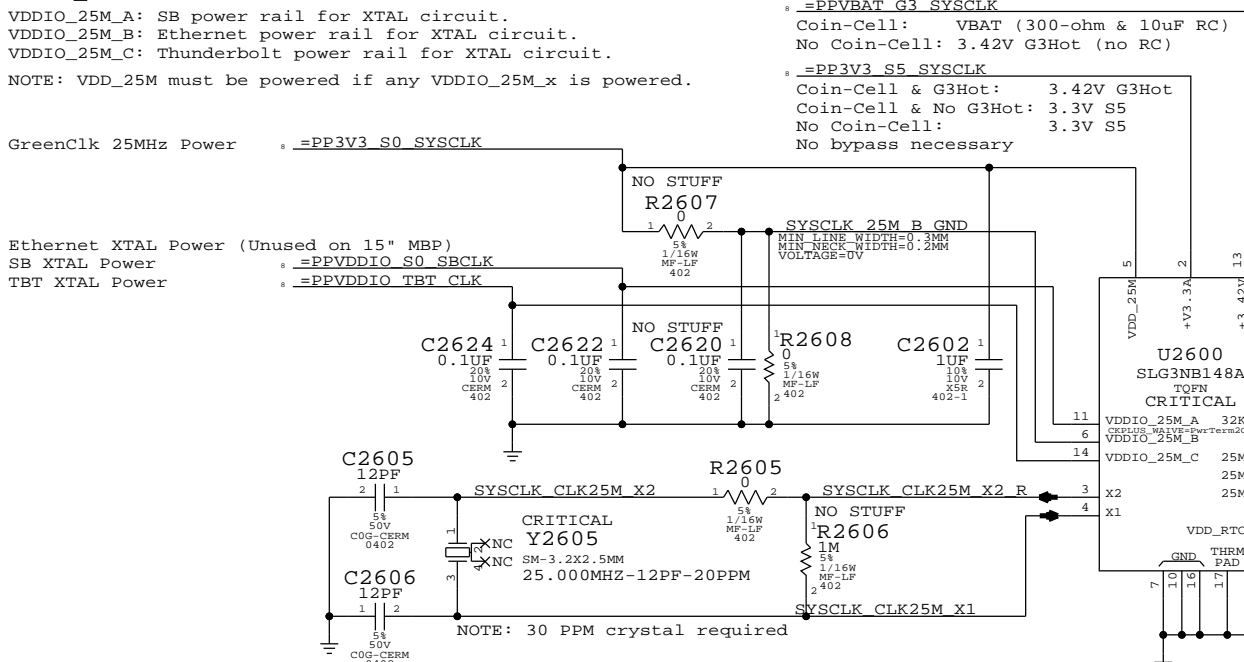
Platform Reset Connections



LPC 33MHz Clock Series Termination

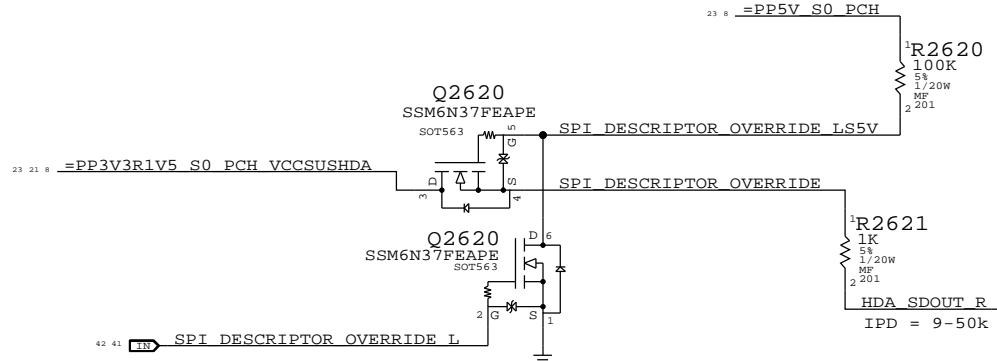



System RTC Power Source & 32kHz / 25MHz Clock Generator



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
Chipset Support			
 Apple Inc.		DRAWING NUMBER	051-9589
		D	
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		26 OF 132	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		25 OF 99	
IV ALL RIGHTS RESERVED			

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

BOM TABLE

PPUSB HUB2 VDD1V8
MIN_LINE_WIDTH=0.4MM
MIN_NCK_WIDTH=0.2MM
VOLTAGE=1.8V

PPUSB HUB2 VDD1V8PLL
MIN_LINE_WIDTH=0.4MM
MIN_NCK_WIDTH=0.2MM
VOLTAGE=1.8V

VDD33

CRPFLT

PLLFILT

SYM VER 1
U2700
USB2513B
QFN

TEST

RESET*

XTALIN/CLKIN

XTALOUT

SUSP_IND/LOCAL_PWR/NON_REMO

SDA/SMBDATA/NON_REM1

SCL/SMBCLK/CFG_SEL0

HS_IND/CFG_SEL1

IPU OCS1*

IPU OCS2*

IPU OSC3*

IPU NC

RBIAS

VBUS_DET

CKPLUS_MAIVE=MidPr_badTerm

USBDM_UP

USBDP_UP

THRM_PAD

1 USBHUB DN1 N

2 USBHUB DN1 P

3 USBHUB DN2 N

4 USBHUB DN2 P

5 USBHUB DN3 N

6 USBHUB DN3 P

7 USBHUB DN4 N

8 USBHUB DN4 P

12 TP USB HUB PRTWPR1

16 NC USB HUB PRTWPR2

18 NC USB HUB PRTWPR3

20 NC USB HUB PRTWPR4

13 TP USB HUB OCS1

17 NC USB HUB OCS2

19 NC USB HUB OCS3

21 NC USB HUB OCS4

27 USB HUB VBUS DET

30 USB HUB UP N

31 USB HUB UP P

PCH PORT 7 (EHC11)

BLUETOOTH FOR 15" MBP & MBP OG

TRACKPAD/KEYBOARD FOR 15" MBP

SMC DEBUG PORT FOR 15" MBP, IR

NC FOR 15" MBP, SMC DEBUG PORT

=PP3V3 S3 USB HUB

R2708

10K

5A

1/16W

NP-LF

402

CRITICAL

R2709

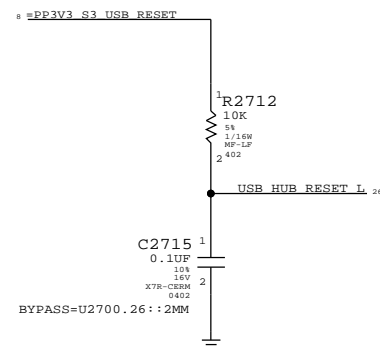
12K

1A

1/16W

NP

402



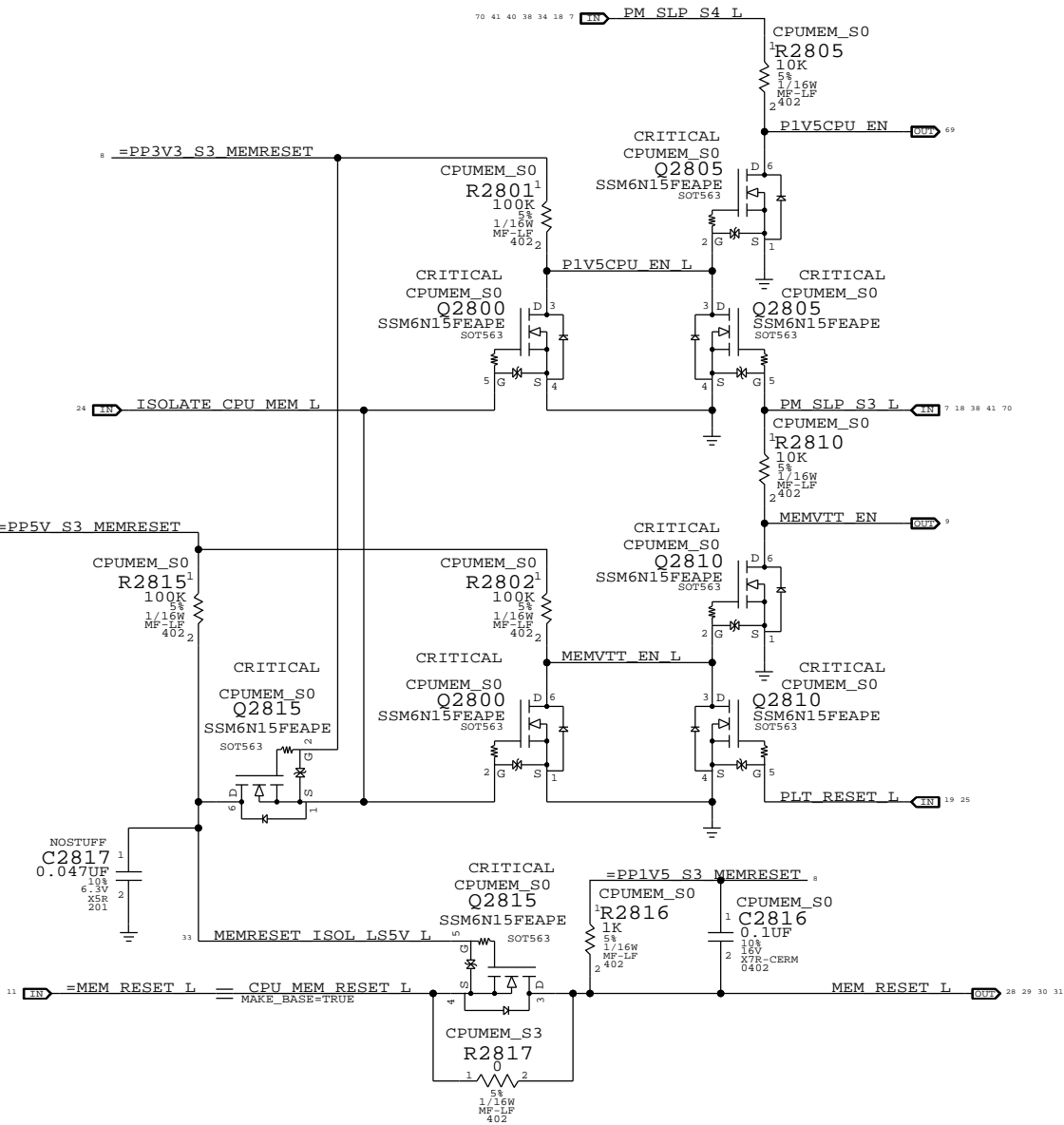
=PP3V3_S3_USBMUX
 C2760 0.1uF
 20E 10V CERAM 402
 VCC
 U2760 PI3USB1022LE 709M CRITICAL
 M+ 5
 M- 4
 D+ 7
 D- 6
 OE* 8
 GND 9
 Y+ 1
 Y- 2
 SEL 10
 USB_EXTB_EHCI_P 19
 USB_EXTB_EHCI_N 91
 USB_EXTB_XHCI_P 19
 USB_EXTB_XHCI_N 91
 USB_EXTB_P 7 38 91
 USB_EXTB_N 7 38 91
 USB_EXTB_SEL_XHCI 17
 TO CONNECTOR
 PULL-UP TO 3.3V SUS ON PCH PAGE, SEL PIN IS LEAKAGE-SOURCE
 PCH GPIO60
 SEL=0 CHOOSE USB EHCI2 PORT
 SEL=1 CHOOSE USB XHCI PORT

A

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

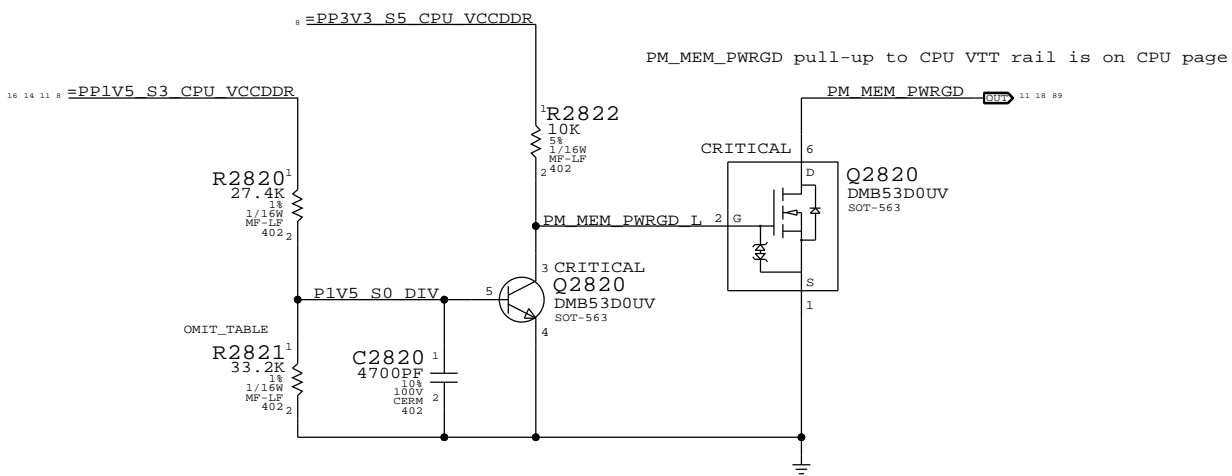
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

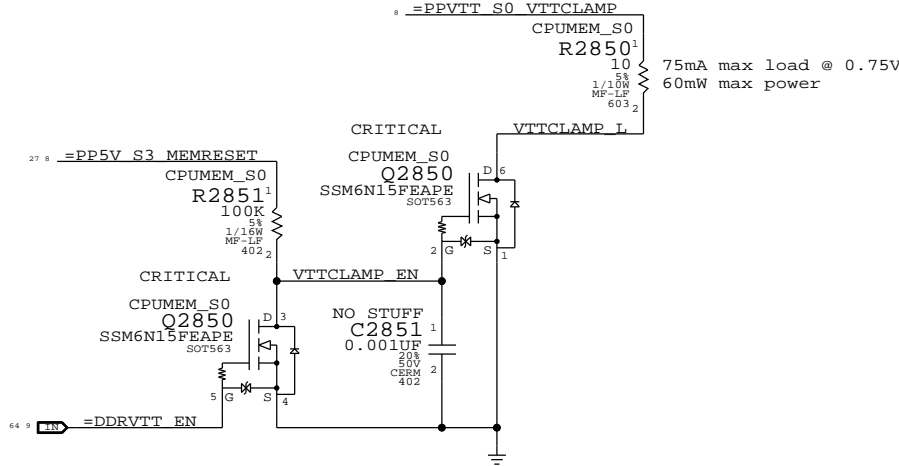


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0365	1	RES,MTL,P15M,1/16W,33,2K,1,0402,SMD,LF	R2821		PPDDR:1V5
114S0376	1	RES,MTL,P15M,1/16W,43,2K,1,0402,SMD,LF	R2821		PPDDR:1V35

1V5 S0 "PGOOD" for CPU




MEMVTT Clamp
Ensures CKE signals are held low in S3

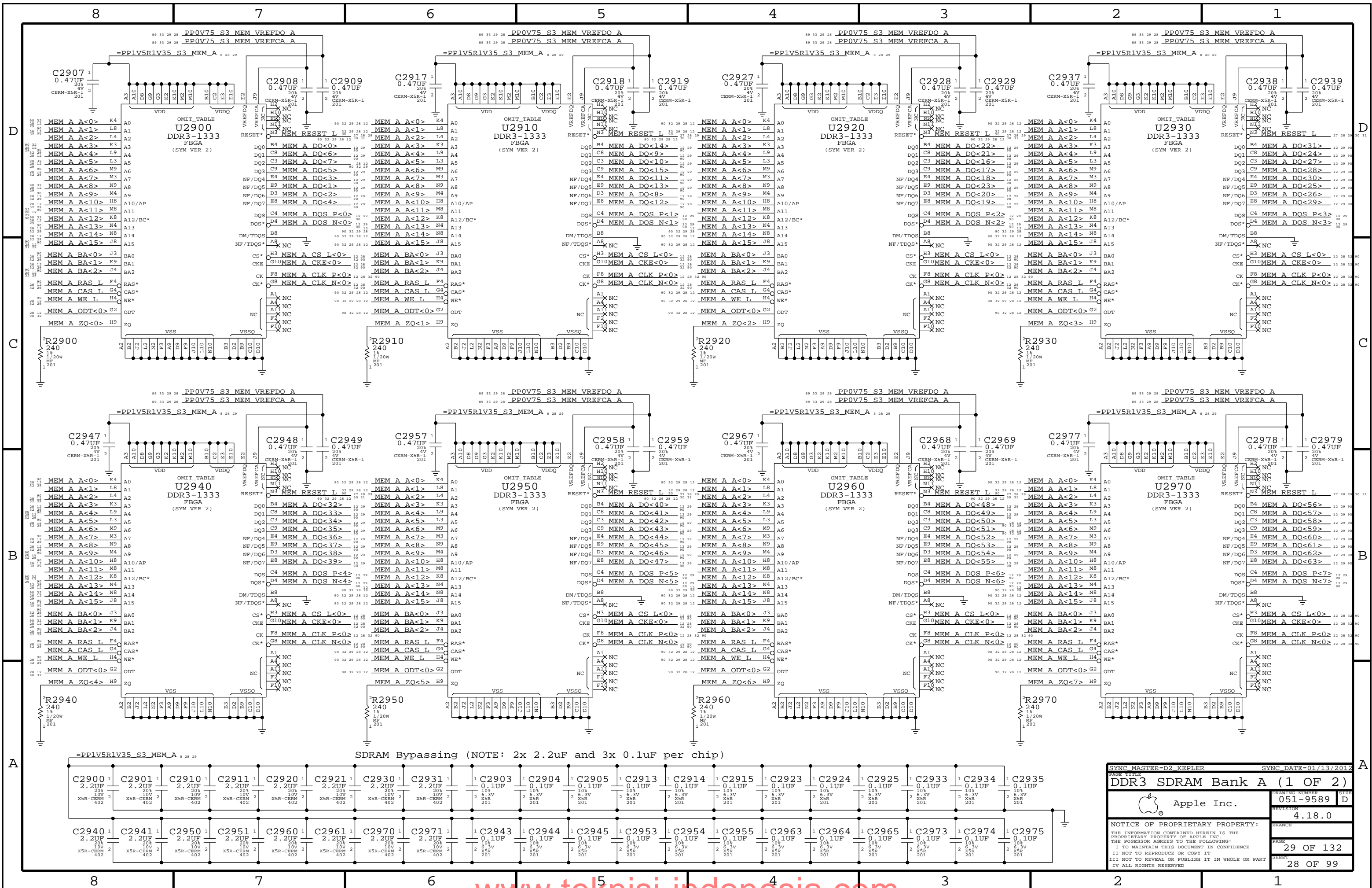


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

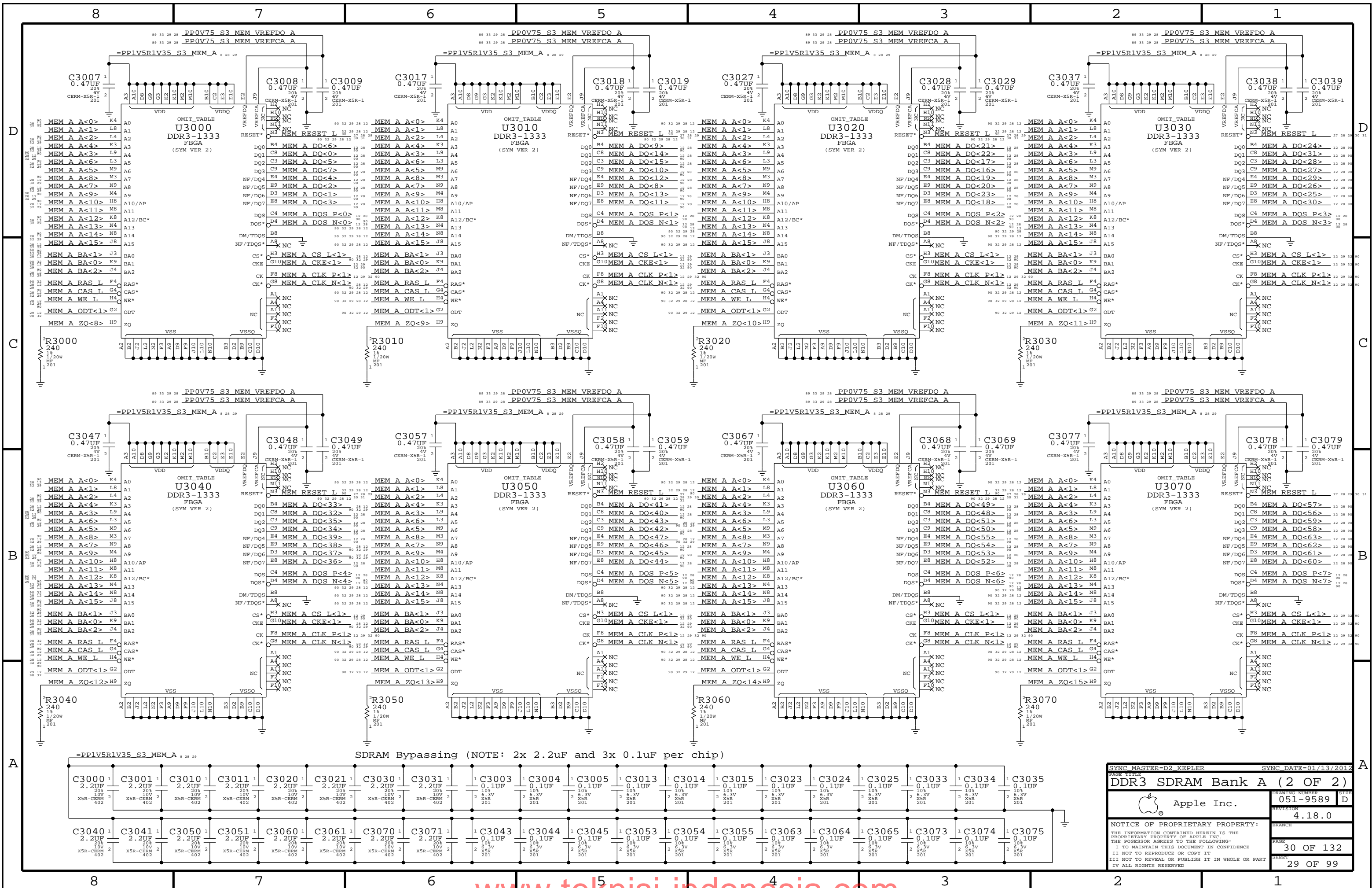
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

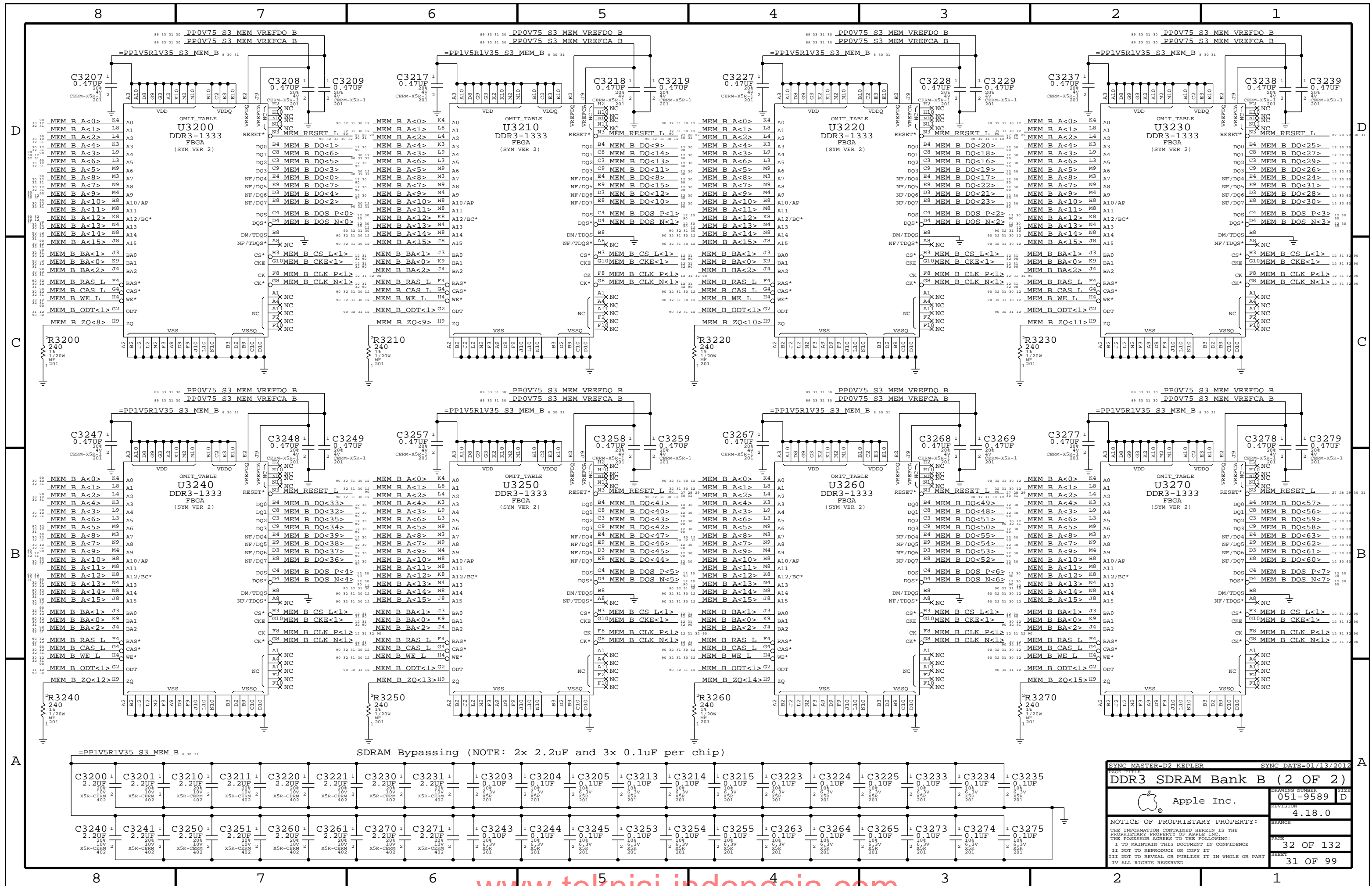
SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
CPU Memory S3 Support		DRAWING NUMBER	
 Apple Inc.		051-9589	SHEET D
		REVISION 4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		28 OF 132	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		27 OF 99	
IV ALL RIGHTS RESERVED			



SYNC MASTER=D2 KEPLER
PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)
Apple Inc.
DRAWING NUMBER
051-9589
REVISION
4.18.0
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED
PAGE
29 OF 132
SHEET
28 OF 99







PAGE TITLE		SYNC DATE=01/13/2012	
DDR3 SDRAM Bank B (2 OF 2)		DRAWING NUMBER	
Apple Inc.		051-9589	
NOTICE OF PROPRIETARY PROPERTY:		REVISION	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		4.18.0	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		BRANCH	
II NOT TO REPRODUCE OR COPY IT		PAGE	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		32 OF 132	
IV ALL RIGHTS RESERVED		SHEET	
		31 OF 99	



D

C

B

A

D

C

B

A

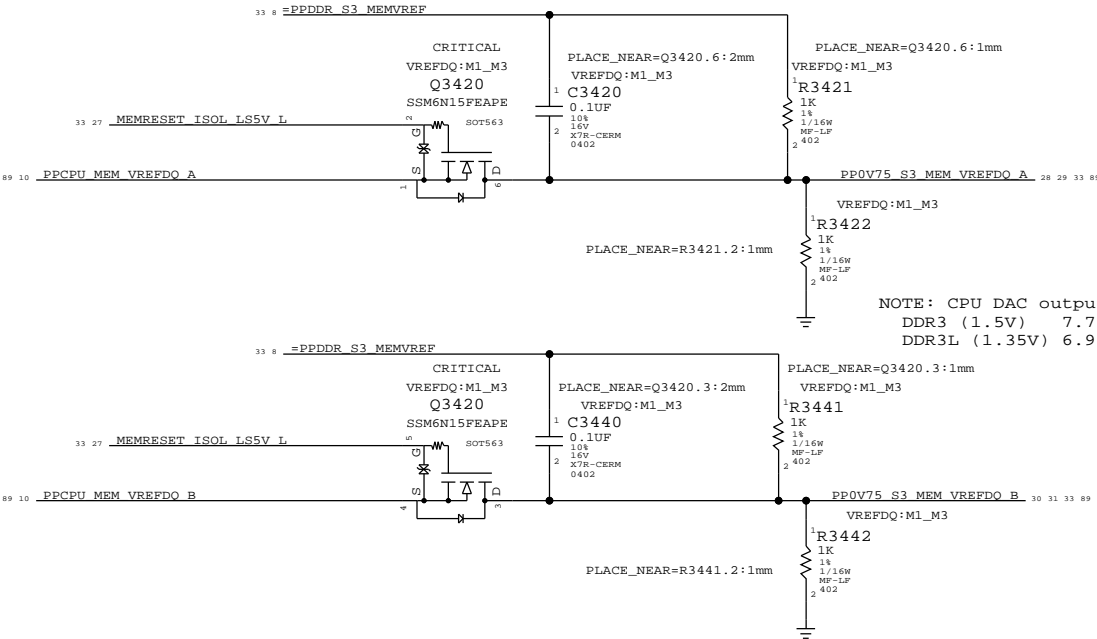
NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.000V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER

051-9589

SIZE

D

REVISION

4.18.0

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

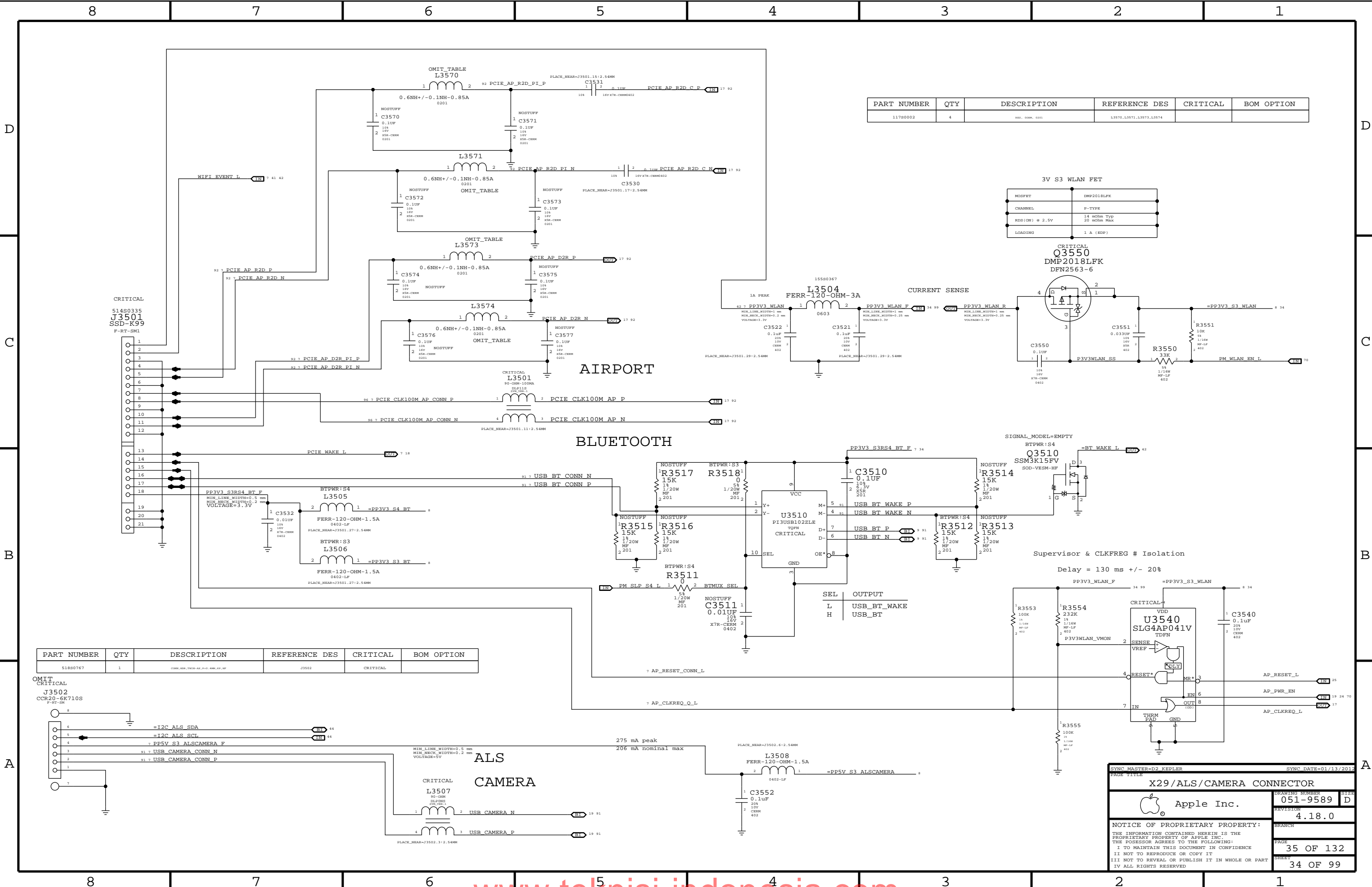
BRANCH

PAGE

34 OF 132

SHEET

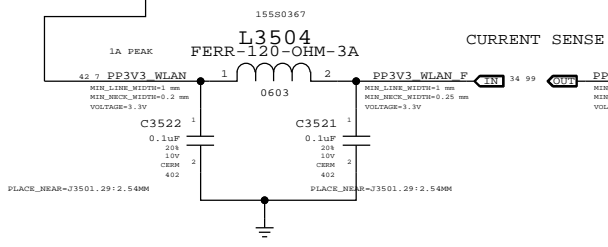
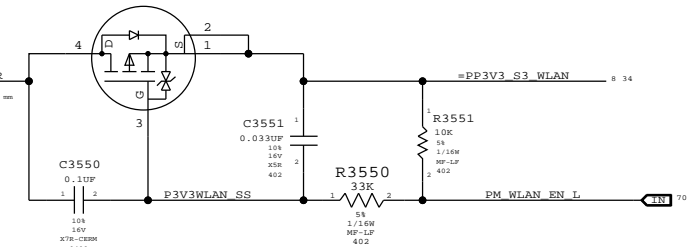
33 OF 99



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	4	88K, 000M, 0201	L3570, L3571, L3573, L3574		

3V S3 WLAN FET	
MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON) @ 2.5V	14 mOhm Typ 20 mOhm Max
LOADING	1 A (EDP)

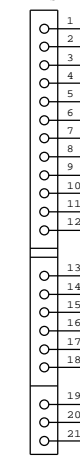
CRITICAL
Q3550
DMP2018LFK
DFN2563-6



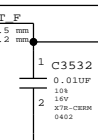
AIRPORT

BLUETOOTH

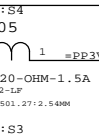
CRITICAL
51480335
J3501
SSD-K99
F-RT-SM1



PP3V3_S3RS4_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V



BTWPR:S4
L3505
G402-LF
PLACE_NEAR=J3501.27:2.54MM
BTWPR:S3
L3506
G402-LF
PLACE_NEAR=J3501.27:2.54MM



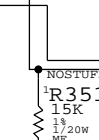
PP3V3_S3_BT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V



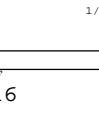
BTWPR:S4
L3505
G402-LF
PLACE_NEAR=J3501.27:2.54MM
BTWPR:S3
L3506
G402-LF
PLACE_NEAR=J3501.27:2.54MM



PP3V3_S3_BT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V



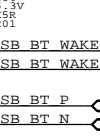
BTWPR:S4
L3505
G402-LF
PLACE_NEAR=J3501.27:2.54MM
BTWPR:S3
L3506
G402-LF
PLACE_NEAR=J3501.27:2.54MM



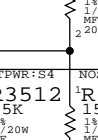
PP3V3_S3_BT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V



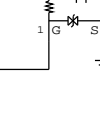
BTWPR:S4
L3505
G402-LF
PLACE_NEAR=J3501.27:2.54MM
BTWPR:S3
L3506
G402-LF
PLACE_NEAR=J3501.27:2.54MM



PP3V3_S3_BT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V



BTWPR:S4
L3505
G402-LF
PLACE_NEAR=J3501.27:2.54MM
BTWPR:S3
L3506
G402-LF
PLACE_NEAR=J3501.27:2.54MM



PP3V3_S3_BT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V



BTWPR:S4
L3505
G402-LF
PLACE_NEAR=J3501.27:2.54MM
BTWPR:S3
L3506
G402-LF
PLACE_NEAR=J3501.27:2.54MM



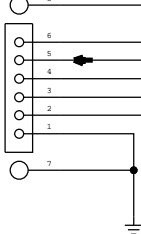
PP3V3_S3_BT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V



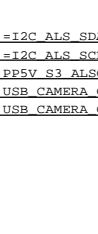
BTWPR:S4
L3505
G402-LF
PLACE_NEAR=J3501.27:2.54MM
BTWPR:S3
L3506
G402-LF
PLACE_NEAR=J3501.27:2.54MM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
51880767	1	CONN, 20P, TYPICAL, 0.5mm, 0.5mm, 0.5mm	J3502	CRITICAL	

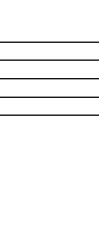
CRITICAL
J3502
CCR20-6K710S
P-RT-001



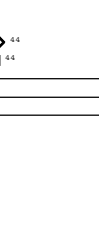
I2C ALS SDA
I2C ALS SCL
PP5V S3 ALS CAMERA F
USB CAMERA CONN N
USB CAMERA CONN P



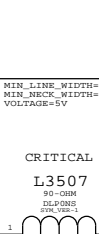
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



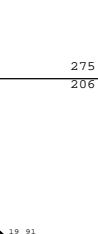
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



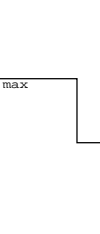
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



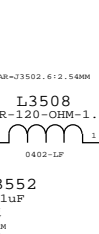
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



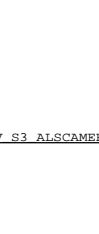
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



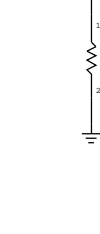
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



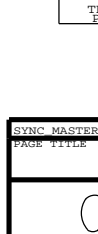
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



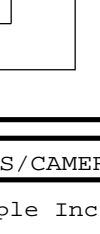
PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V




PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V



PP5V S3 ALS CAMERA F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
X29/ALS/CAMERA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-9589
		SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	4.18.0
		BRANCH	
		PAGE	35 OF 132
		SHEET	34 OF 99



D

C

B

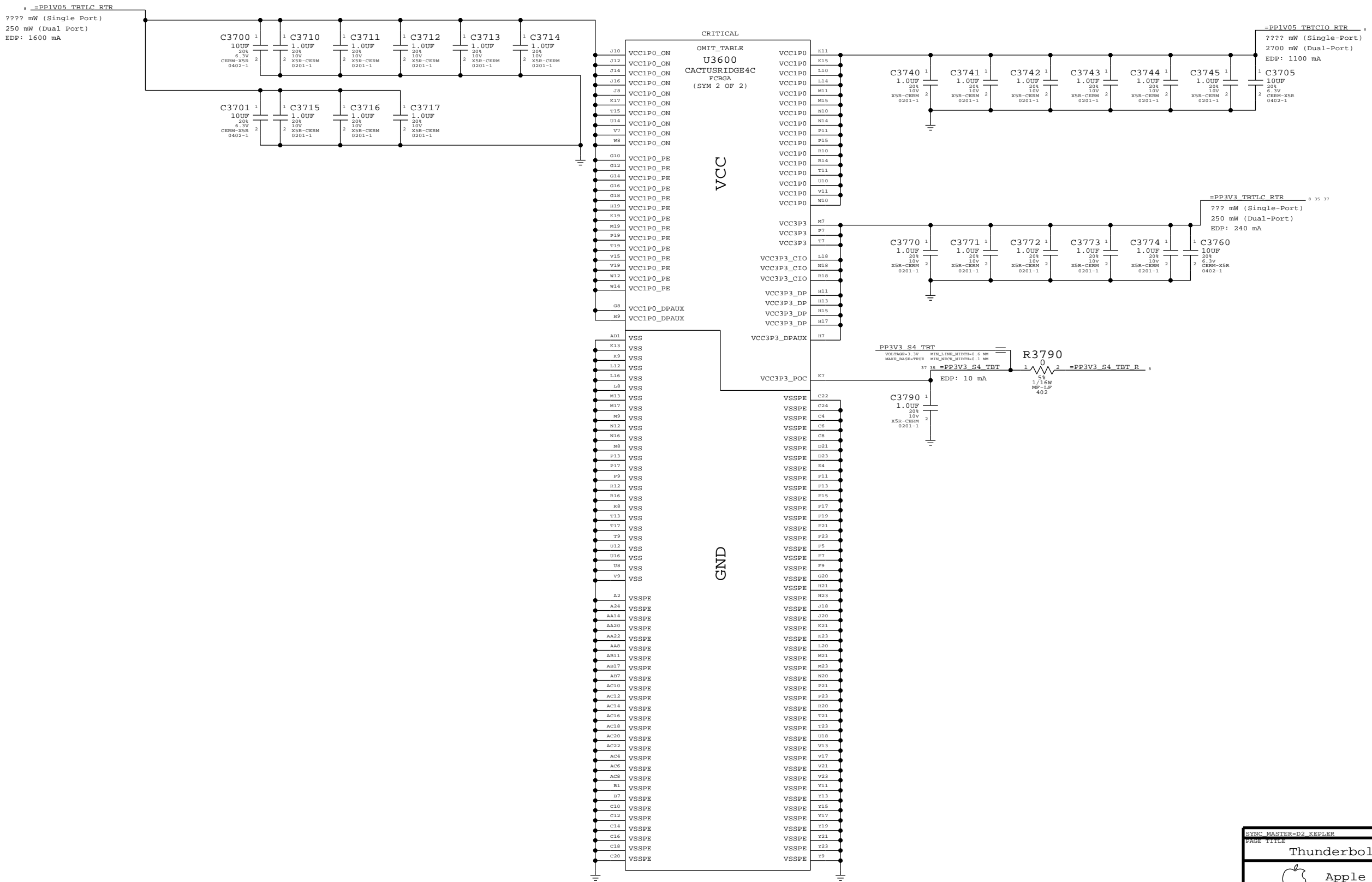
A


D

C

B

A



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
Thunderbolt Host (2 of 2)			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE D
	REVISION	4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		37 OF 132	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		36 OF 99	
IV ALL RIGHTS RESERVED			

Page Notes

Power aliases required by this page:

- PPVIN_SW_TBTBST (8-13V Boost Input)
- PP15V_TBT_REG (15V Boost Output)
- PP3V3_TBT_P3V3TBTFTET (3.3V FET Input)
- PP3V3_TBTLC_FET (3.3V FET Output)
- PP3V3_S0_TBTWRCCTL
- PP1V05_TBT_P1V05TBTFTET (1.05V FET Input)
- PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:

- TBT_CLKREQ_L
- TBT_RESET_L

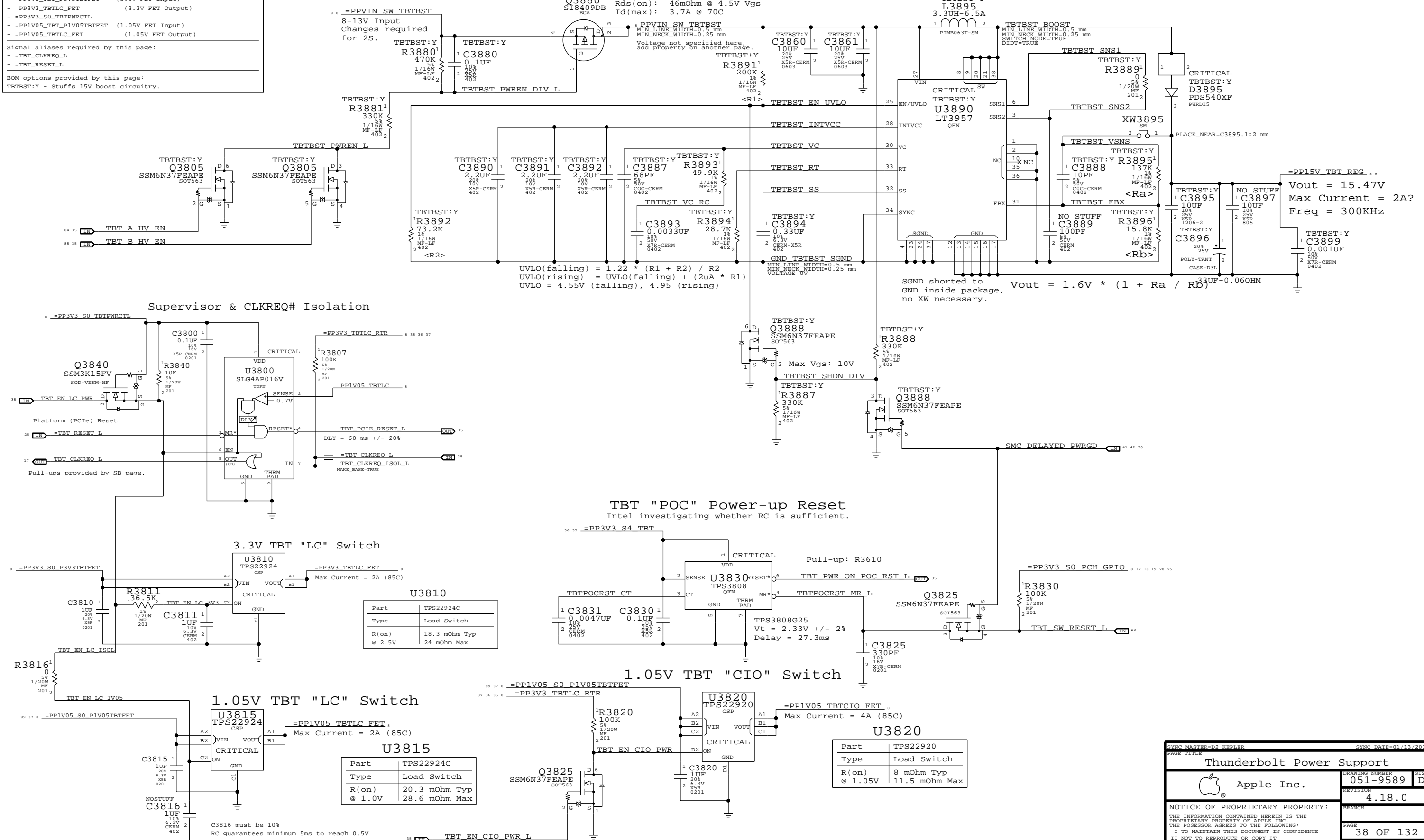
BOM options provided by this page:

TBTBST:Y - Stuffs 15V boost circuitry.

Thunderbolt 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL
TBTBST:Y
L3895
3.3UH-6.5A



D

C

B

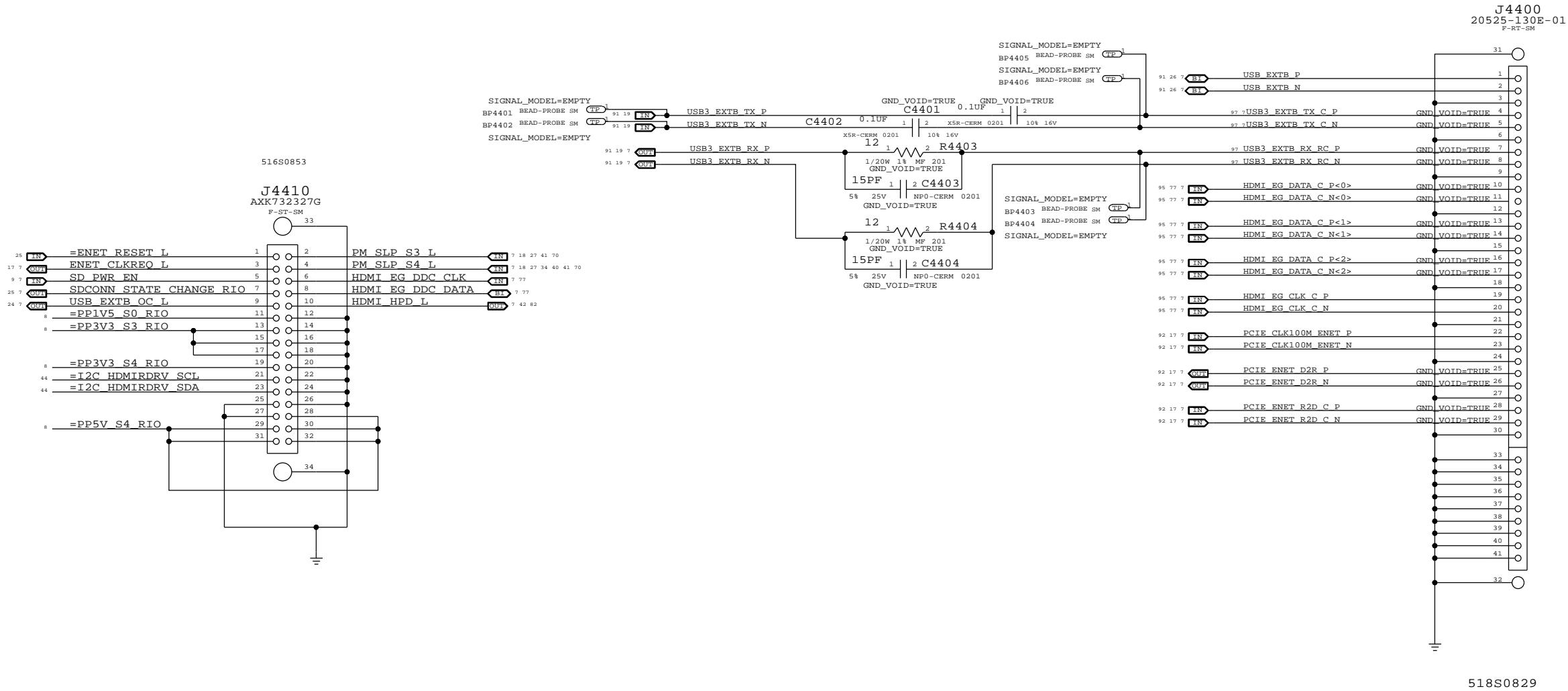
A


D

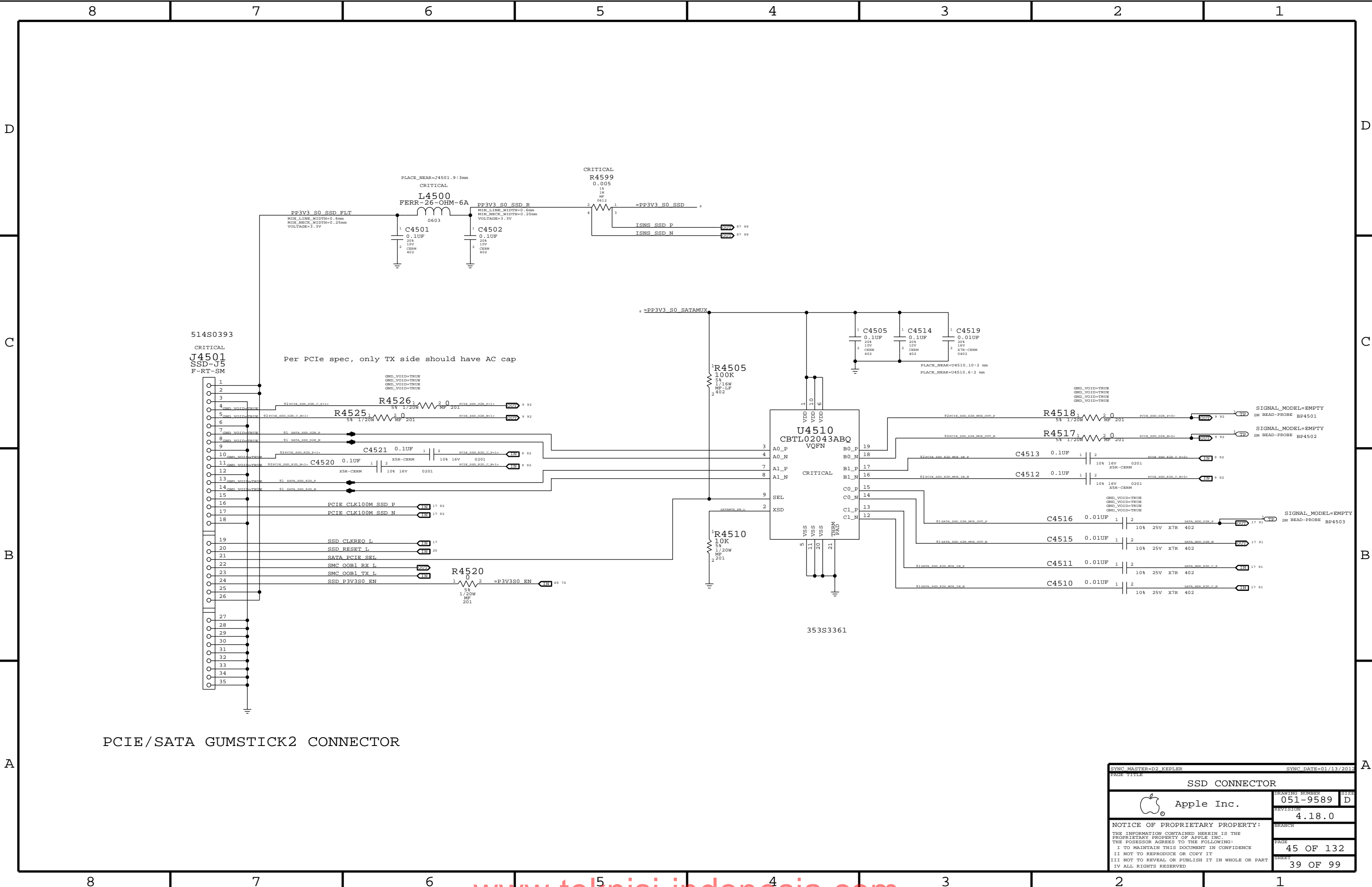
C

B


A

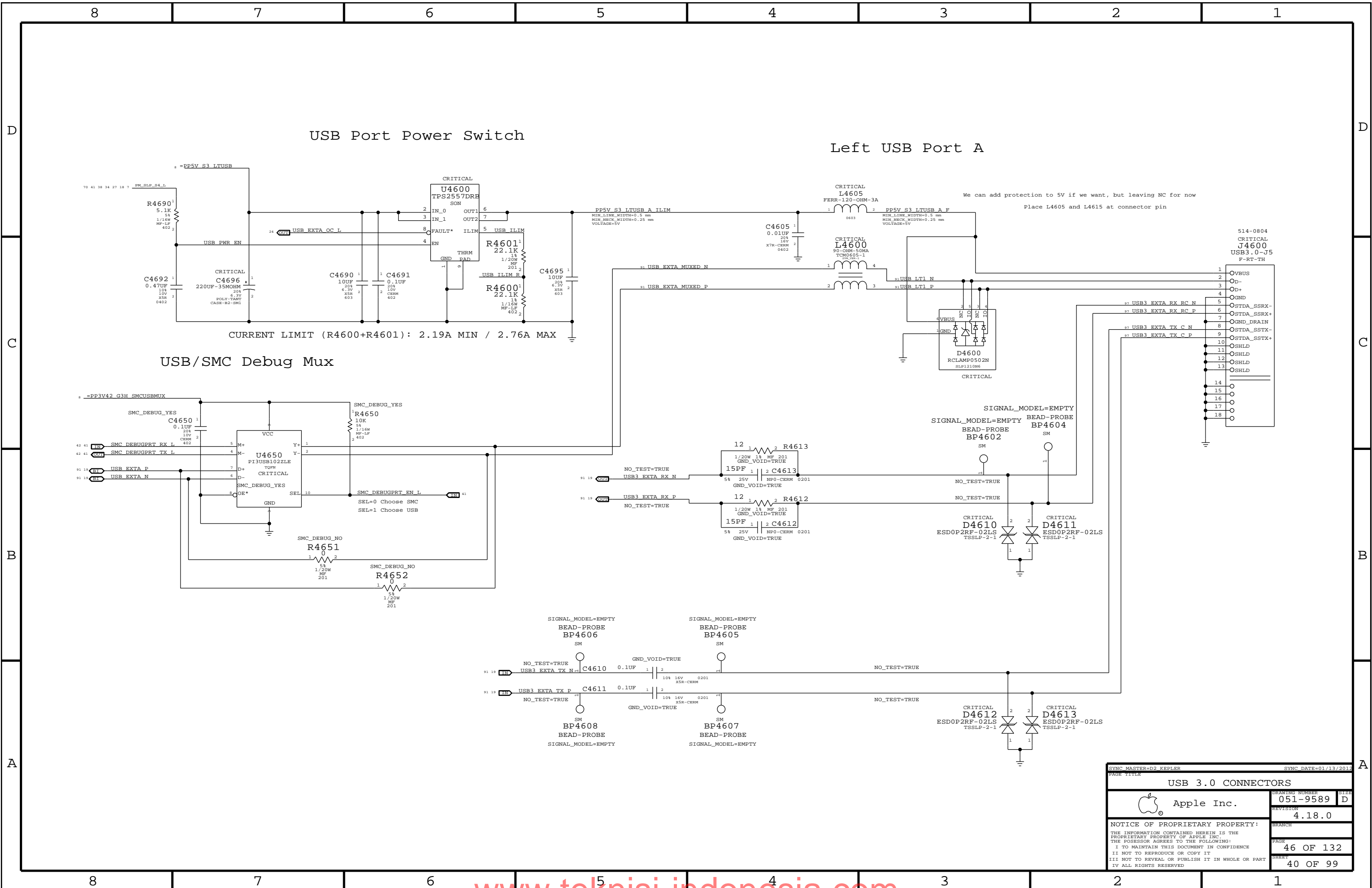



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
RIO CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-9589
		SIZE	D
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
		PAGE	44 OF 132
		SHEET	38 OF 99

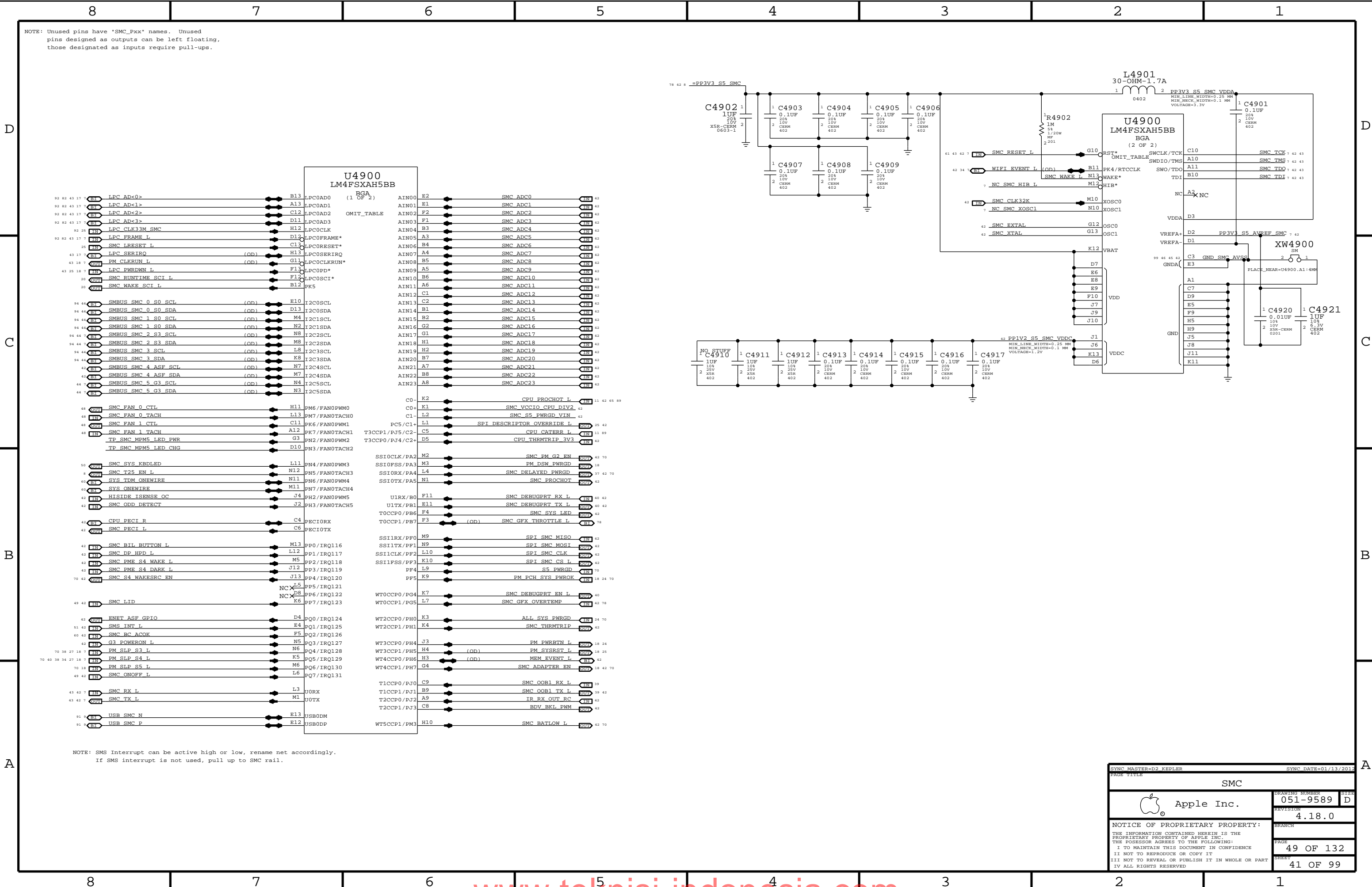


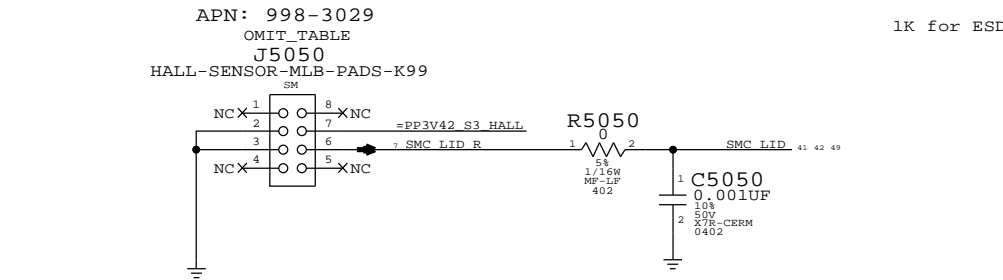
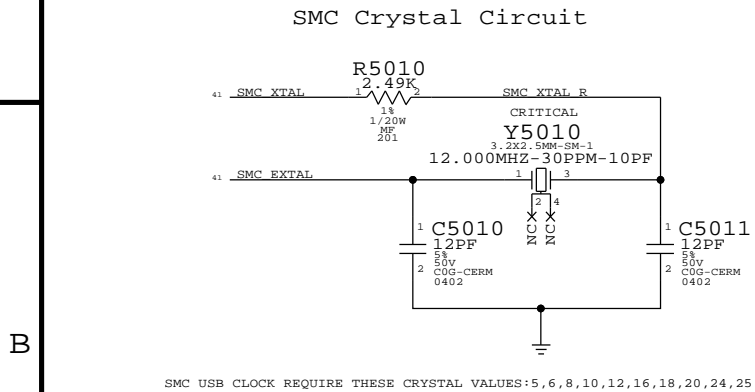
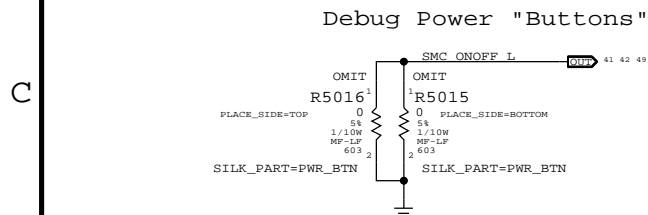
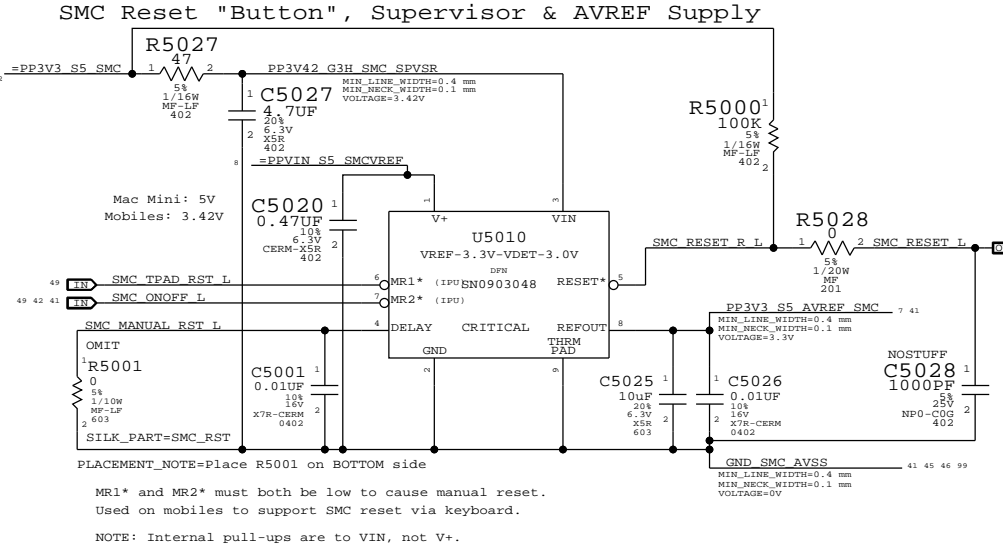
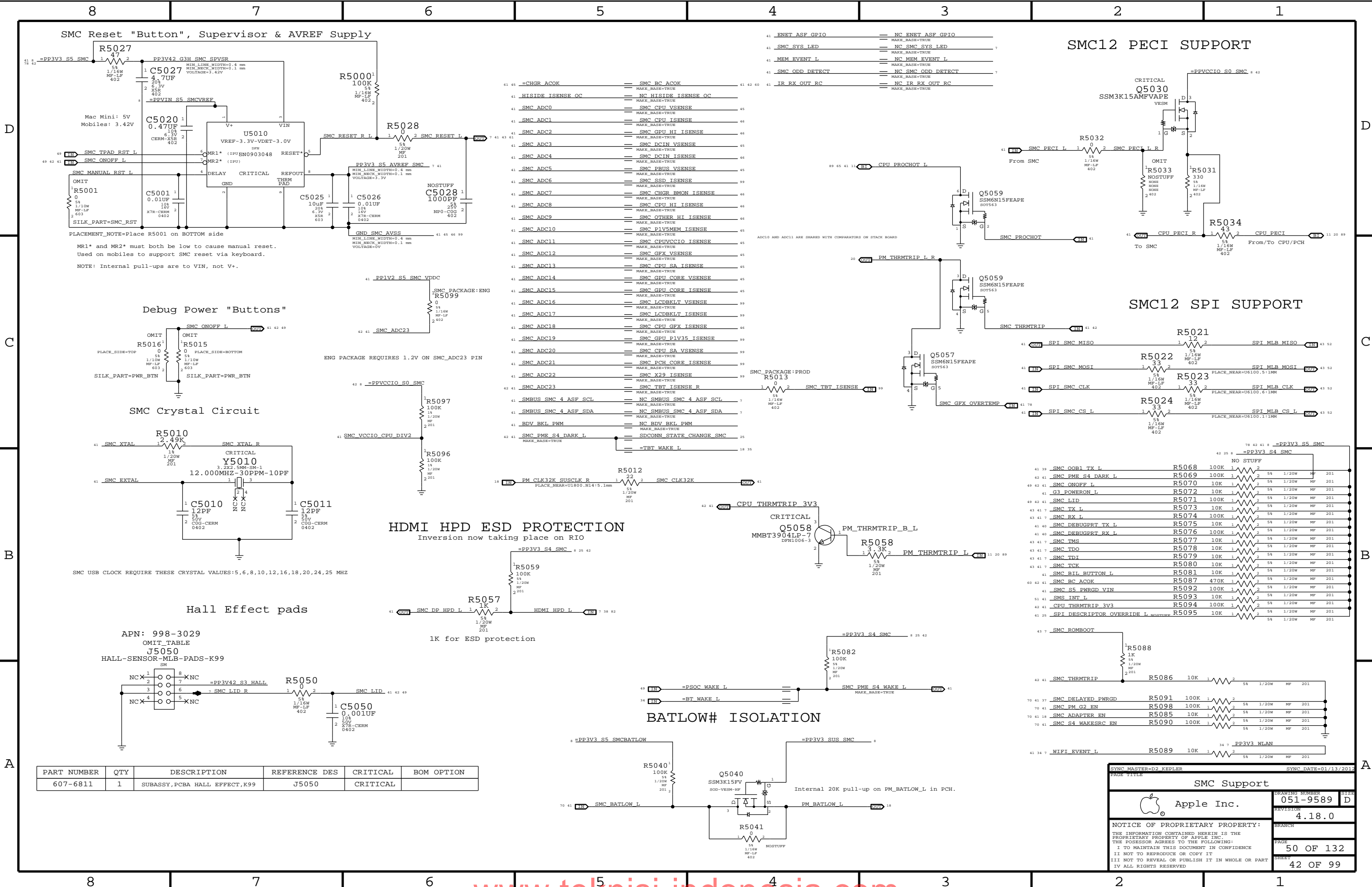
PCIE/SATA GUMSTICK2 CONNECTOR

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
SSD CONNECTOR			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE D
	REVISION	4.18.0	
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			PAGE 45 OF 132
			SHEET 39 OF 99

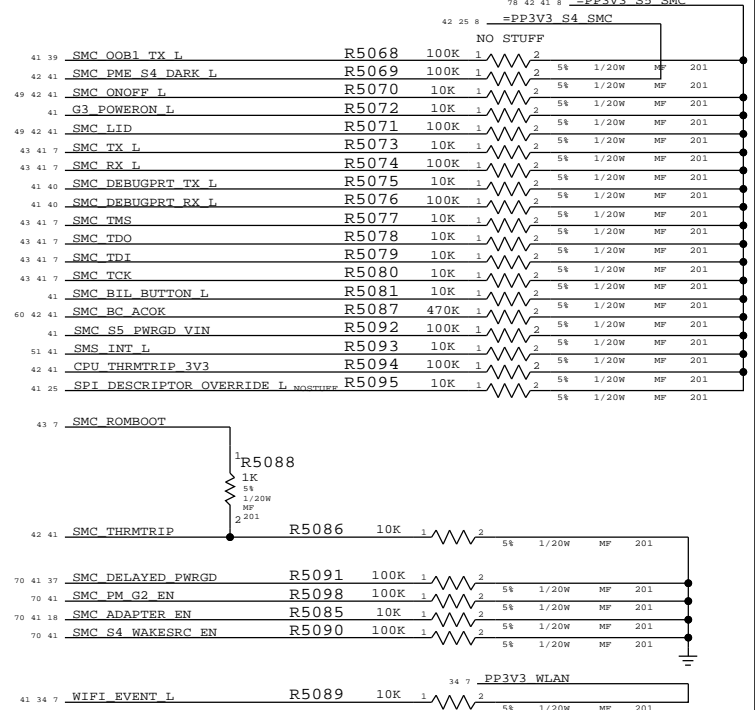
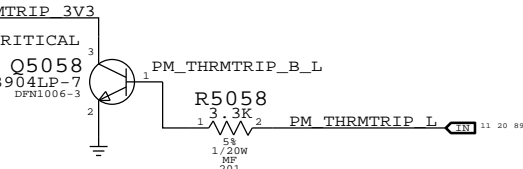
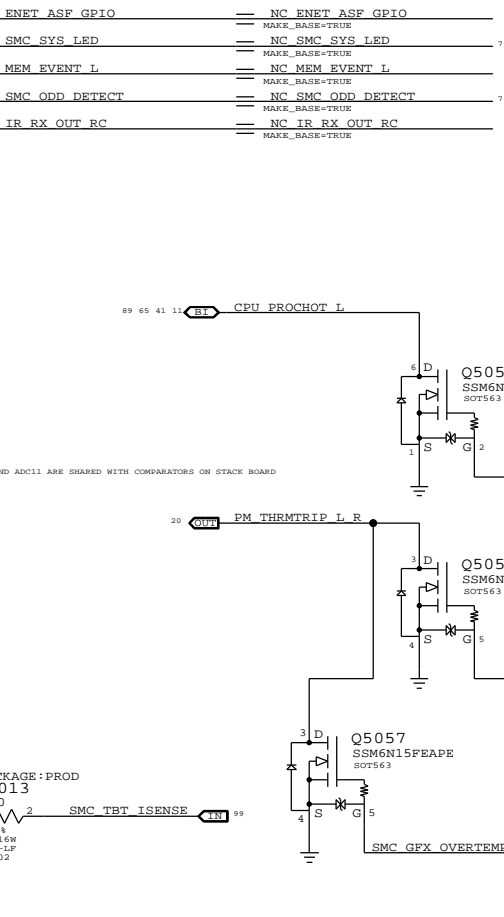
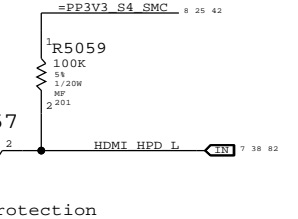
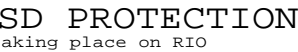
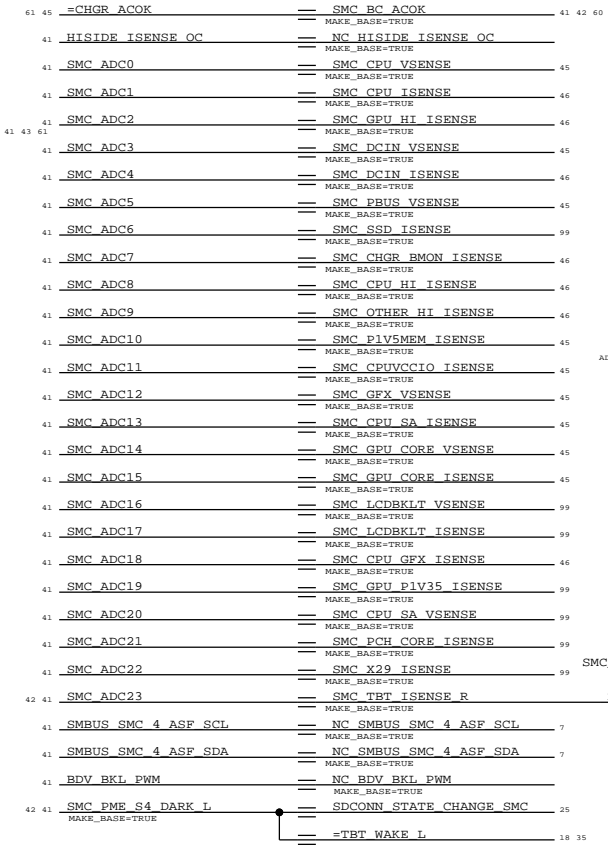


SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
USB 3.0 CONNECTORS			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE
	REVISION	4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	46 OF 132
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	40 OF 99
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5050	CRITICAL	



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
SMC Support		DRAWING NUMBER	051-9589
Apple Inc.		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	50 OF 132
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	42 OF 99
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

D

C

B

A

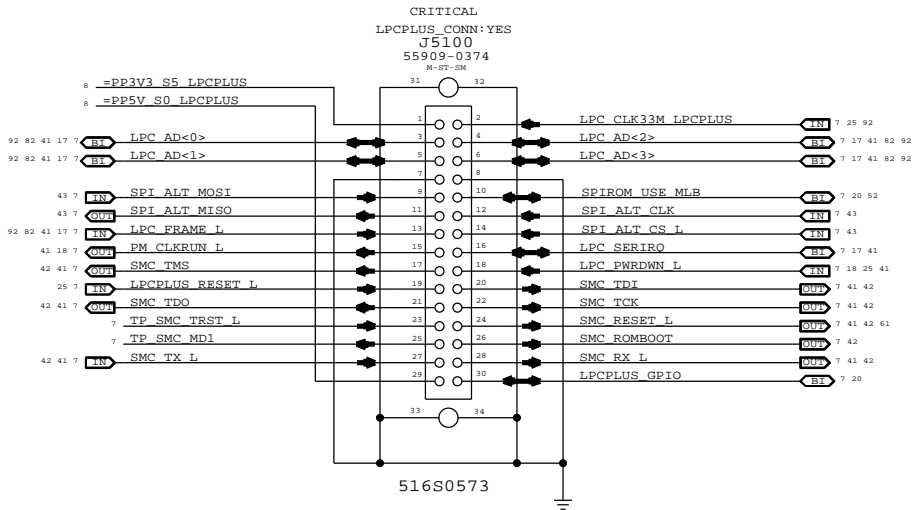
D

C

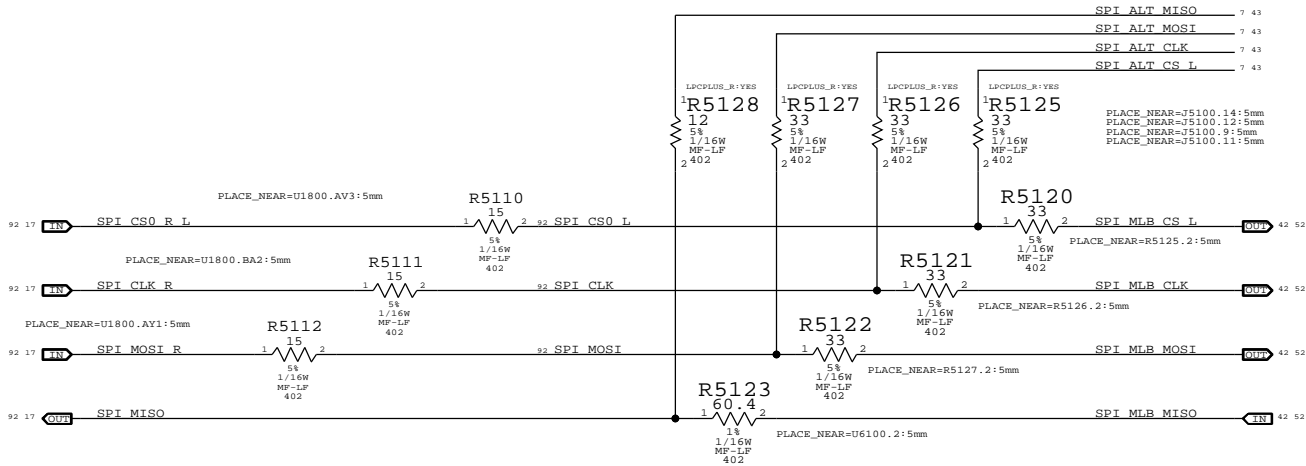
B


A

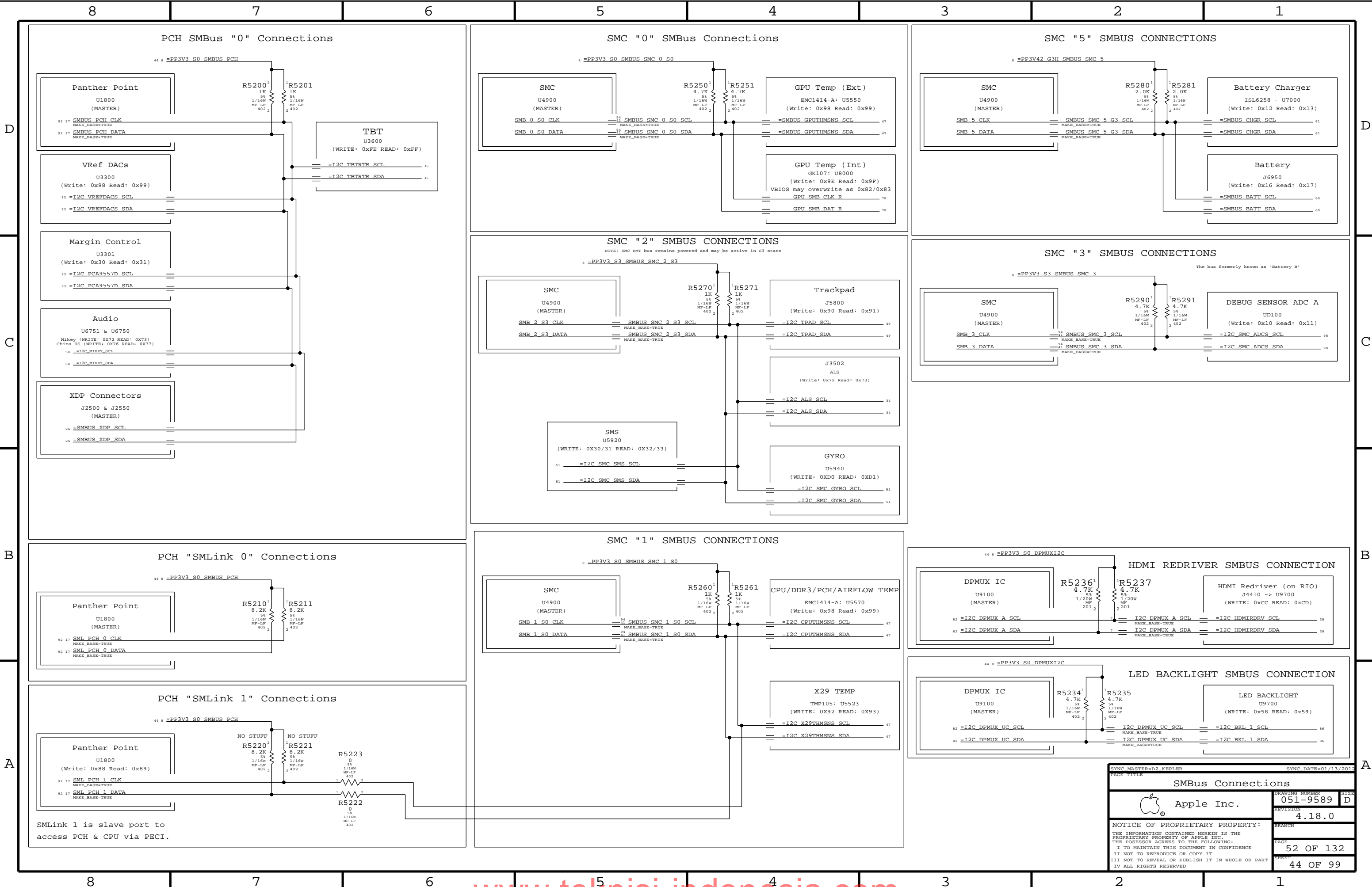
LPC+SPI Connector

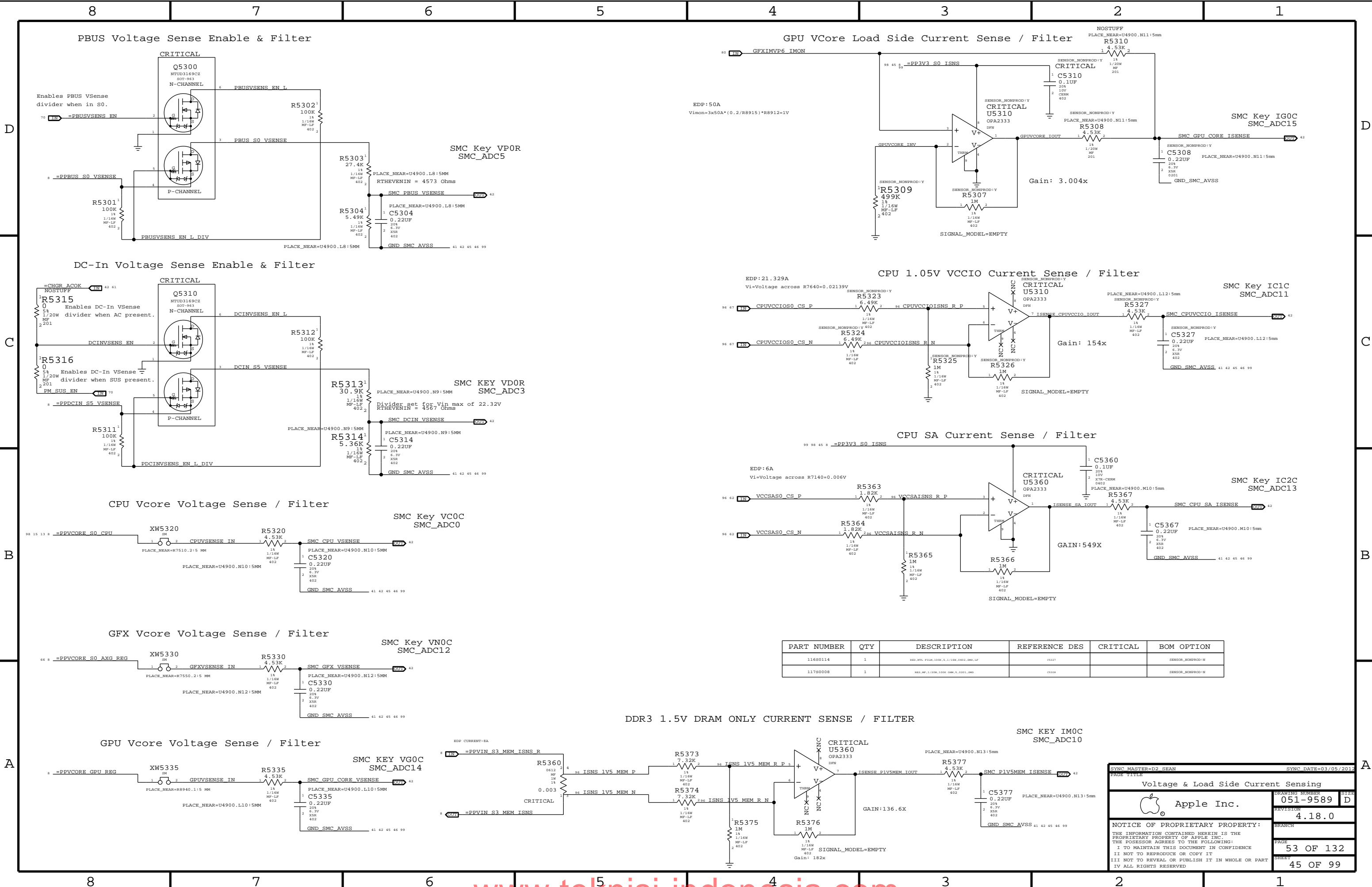


SPI Bus Series Termination



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
LPC+SPI Debug Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9589		D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION		PAGE
	4.18.0		51 OF 132
BRANCH		SHEET	
		43 OF 99	





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680114	1	RES,HTL,P100A,100K,5,1/16W,0402,0MD,LP	C5127		SENSOR_NONPROD:Y
11780008	1	RES,MP,1/20W,100K,0805,5,0201,0MD	C5338		SENSOR_NONPROD:Y

SYNC MASTER=D2 SEAN

SYNC DATE=03/05/2012

Voltage & Load Side Current Sensing

Apple Inc.

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

051-9589

REVISION

4.18.0

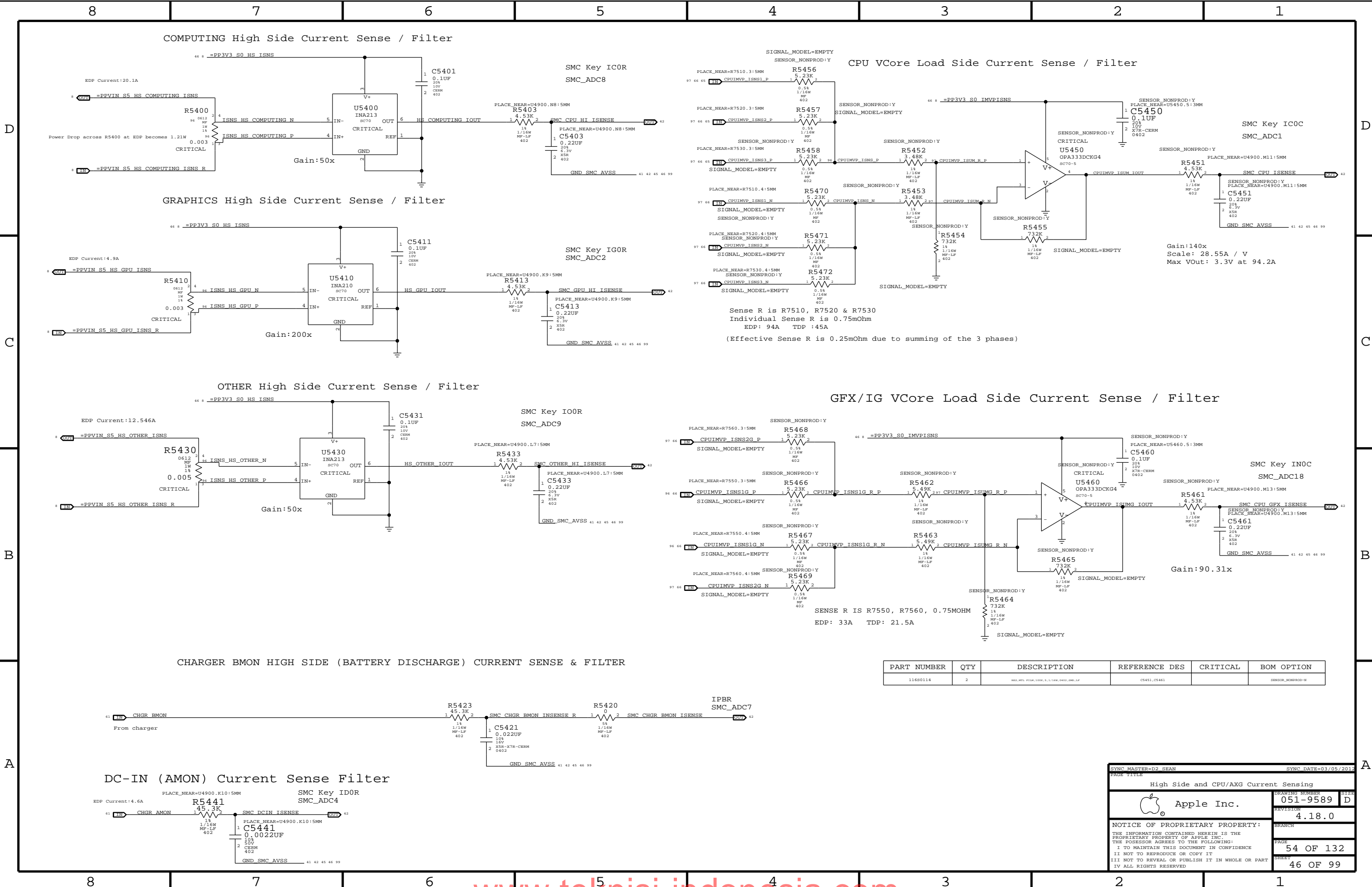
PAGE

53 OF 132

SHEET

45 OF 99

www.teknisi-indonesia.com




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680114	2	RES,MTL,PT100,100K,5,1/16W,0402,080D,LF	C5451,C5451		SENSOR_NONPROD:N

SYNC MASTER=D2 SEAN

SYNC DATE=03/05/2012

PAGE TITLE

High Side and CPU/AXG Current Sensing

 Apple Inc.

DRAWING NUMBER
051-9589

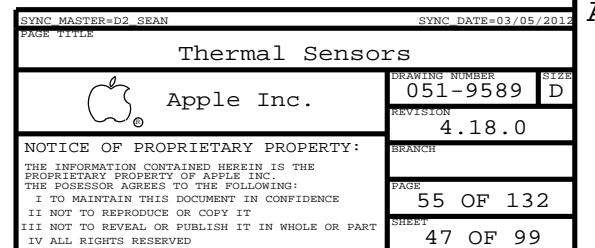
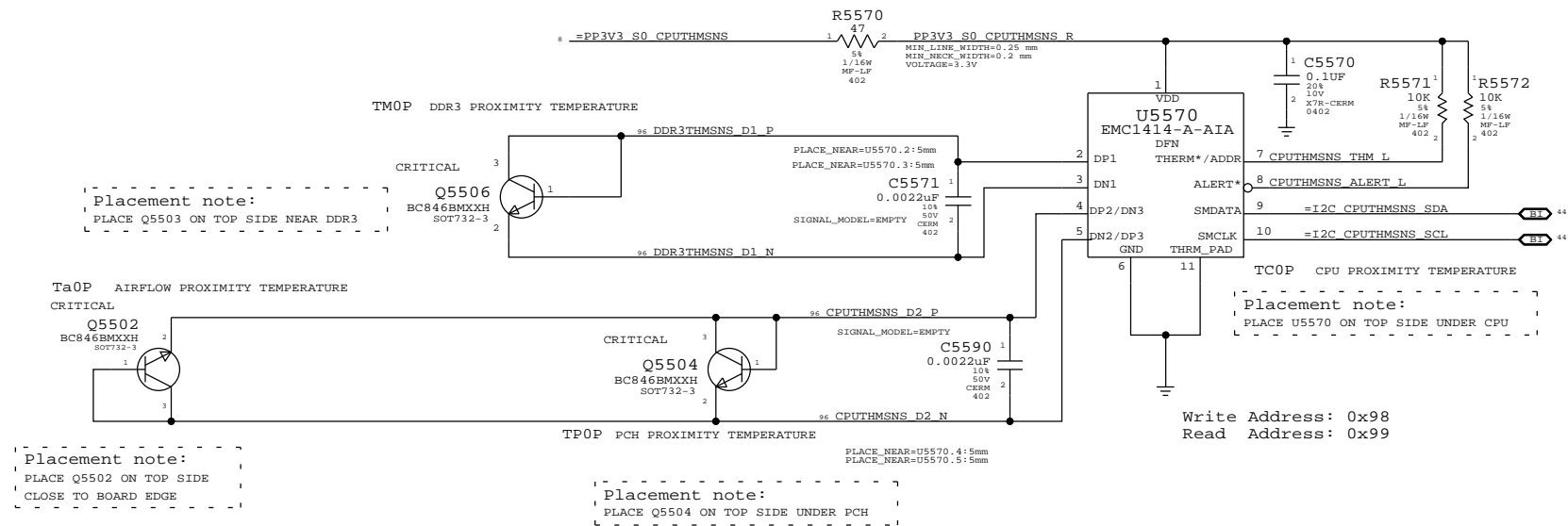
REVISION
4.18.0

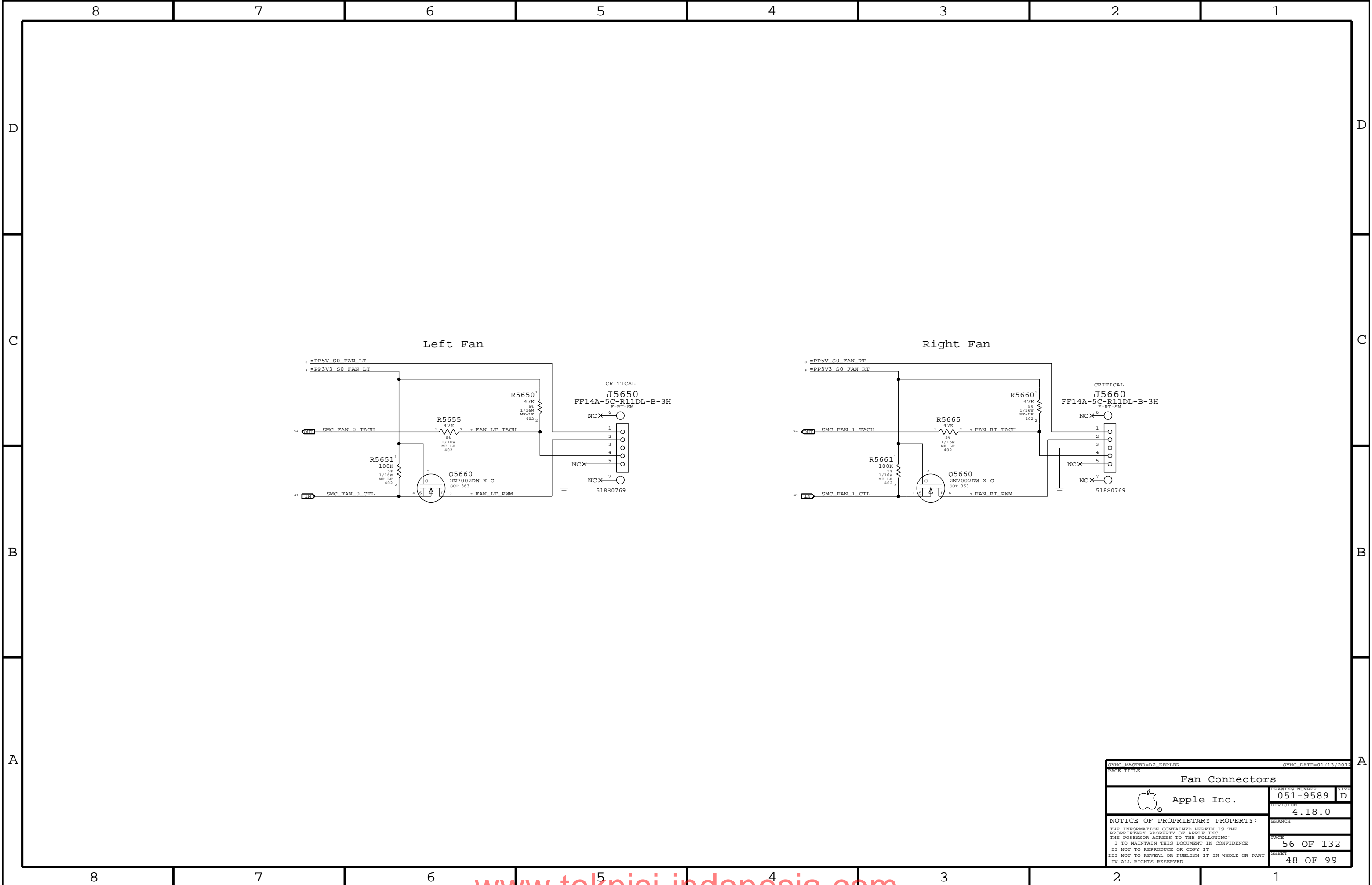
BRANCH

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE
54 OF 132

SHEET
46 OF 99

[illegible]



- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

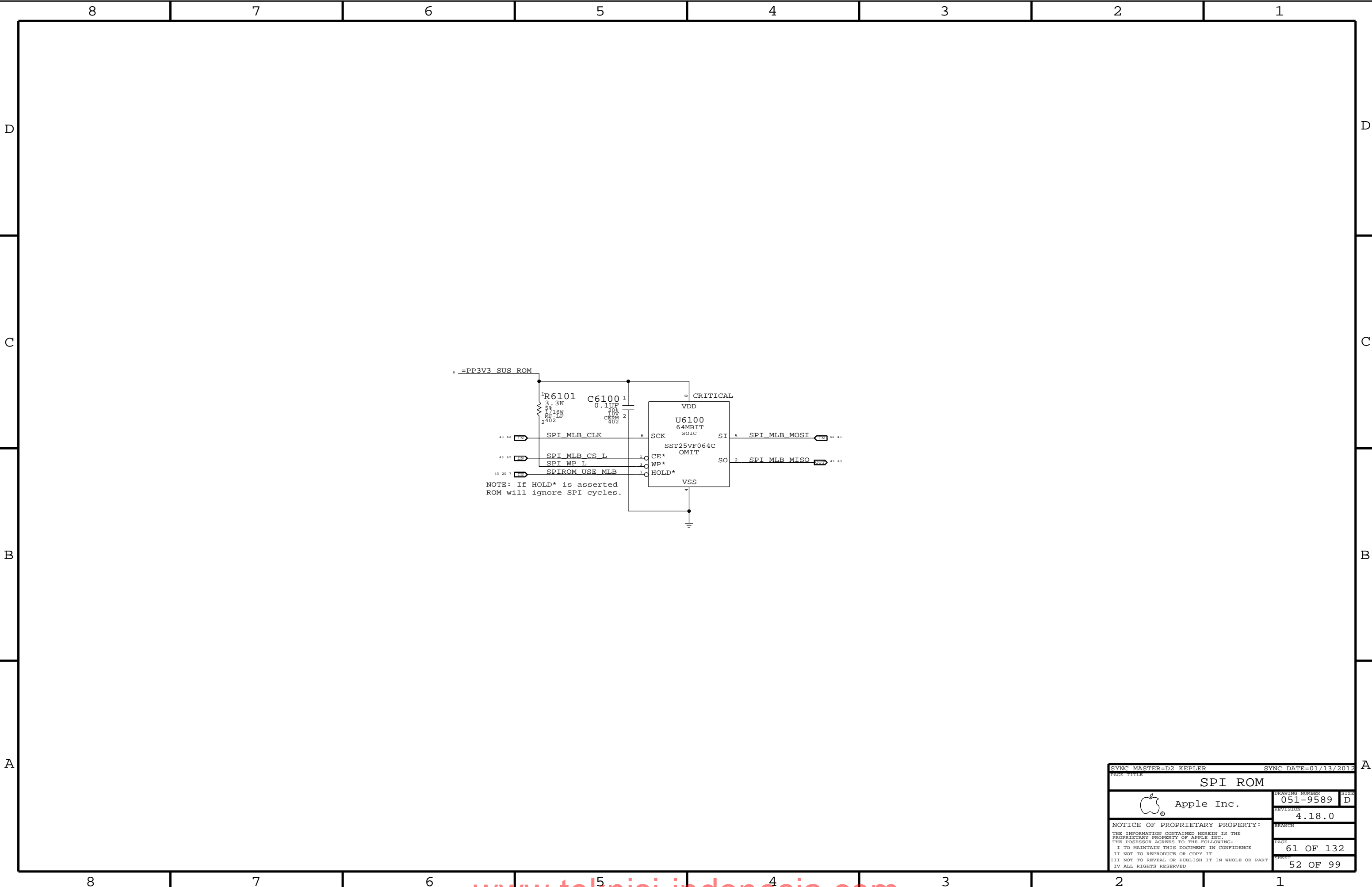
```


nm
R5708
49  # =PP3V3 S4 TPAD 1 0 2
                                5%
                                1/20W
                                MF
                                201
                                NOSTUFF
                                C5708
                                0.1UF
                                1 10%
                                2 6-3V
                                XSR
                                201
                                GND
                                49 7  Z2 CS L
                                VOLTAGE=3.3V
                                MIN_NECK_WIDTH=0.25MM
                                MIN_LINE_WIDTH=0.15MM
                                PP3V3 TPAD 0
                                49 7  Z2 MOSI
                                49 7  Z2 MISO
                                49 7  Z2 SCLK
                                FERR-120-OHM-1.5A
                                L5700
                                PLACE_NEAR=J5800.18:3MM
                                TPAD 5V_SW_S4
                                0402-LF
                                1 2
                                PP5V S4 CUMULUS
                                VOLTAGE=5V
                                MIN_NECK_WIDTH=0.20MM
                                MIN_LINE_WIDTH=0.50MM
                                49 7  Z2 HOST I
                                49 7  Z2 CLKIN
                                R5700
                                220K
                                5%
                                1/20W
                                MF
                                201
                                # =PP5V S4 TPAD 1 2
                                1 0402-LF
                                2 TPAD 5V_SW_S4
                                1 C5700
                                0.1UF
                                2 10%
                                15V PLACE_NEAR=J5800.18:3MM
                                XSR-CERM
                                0201
                                GND
                                TPAD 5V_LDO
                                PLACE_NEAR=J5800.18:3MM
                                L5707
                                FERR-120-OHM-1.5A
                                49 7  Z2 CS L
                                49 7  Z2 MOSI
                                49 7  Z2 MISO
                                49 7  Z2 SCLK
                                49 7  Z2 HOST I
                                49 7  Z2 CLKIN
                                R5700
                                220K
                                5%
                                1/20W
                                MF
                                201
                                # =PP5V S5RS4 CUMULUS 1 2

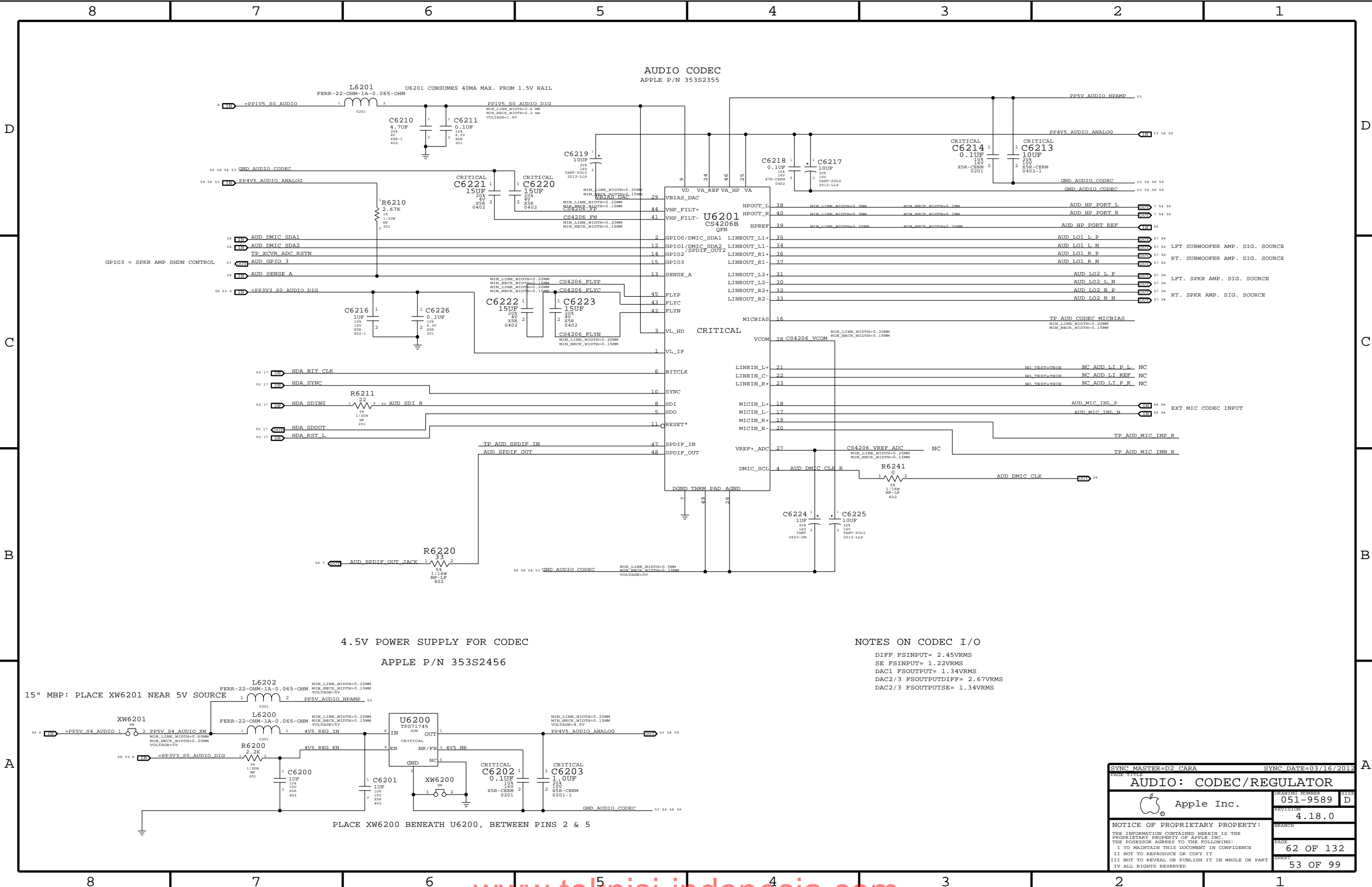
```

IPD Flex Connector





SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
SPI ROM			
 Apple Inc.		DRAWING NUMBER	
		051-9589	
		D	
		REVISION	
		4.18.0	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.			
THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
		BRANCH	
		PAGE	
		61 OF 132	
		SHEET	
		52 OF 99	



D

C

B

A

D

C

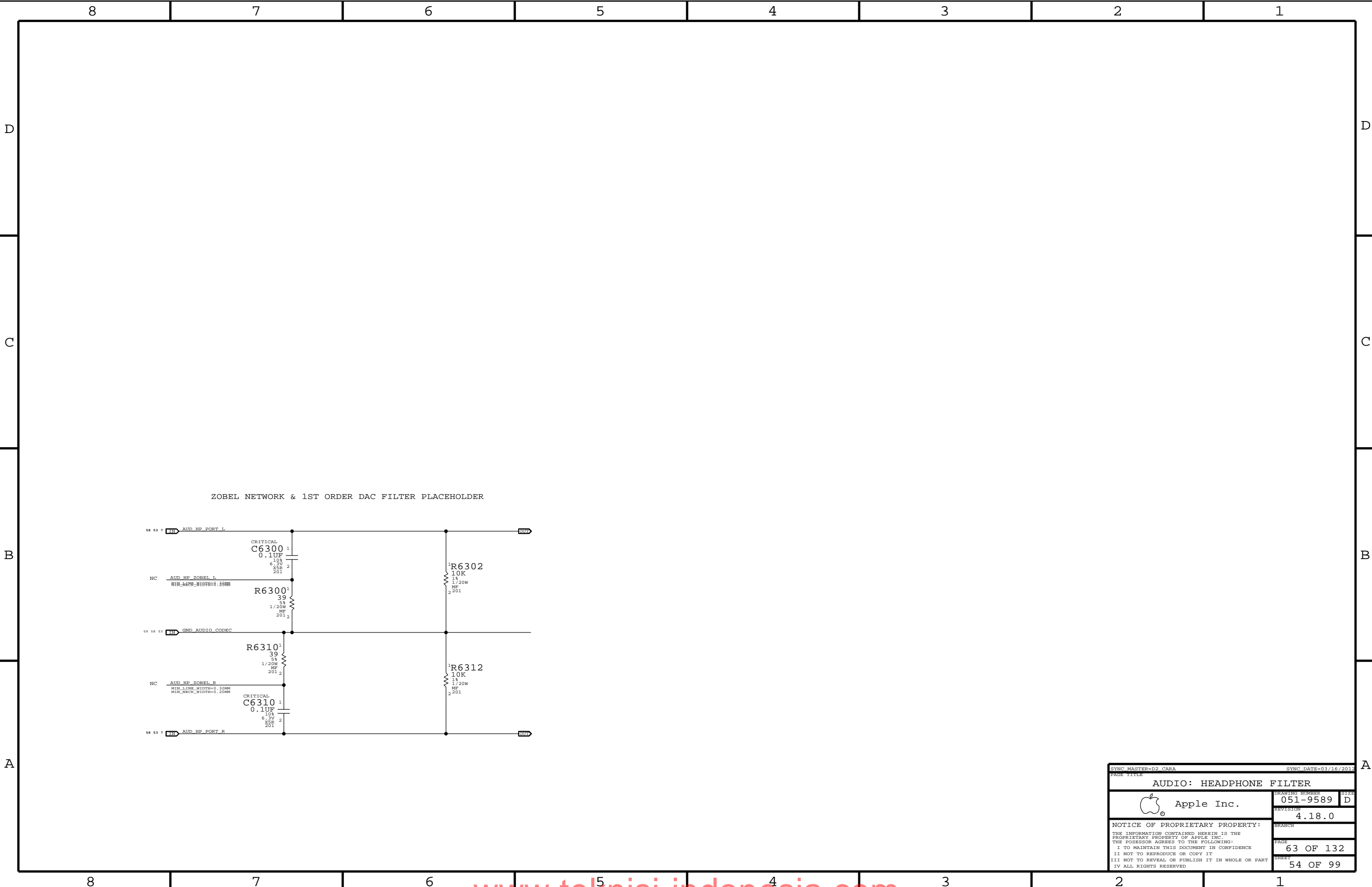
B


A

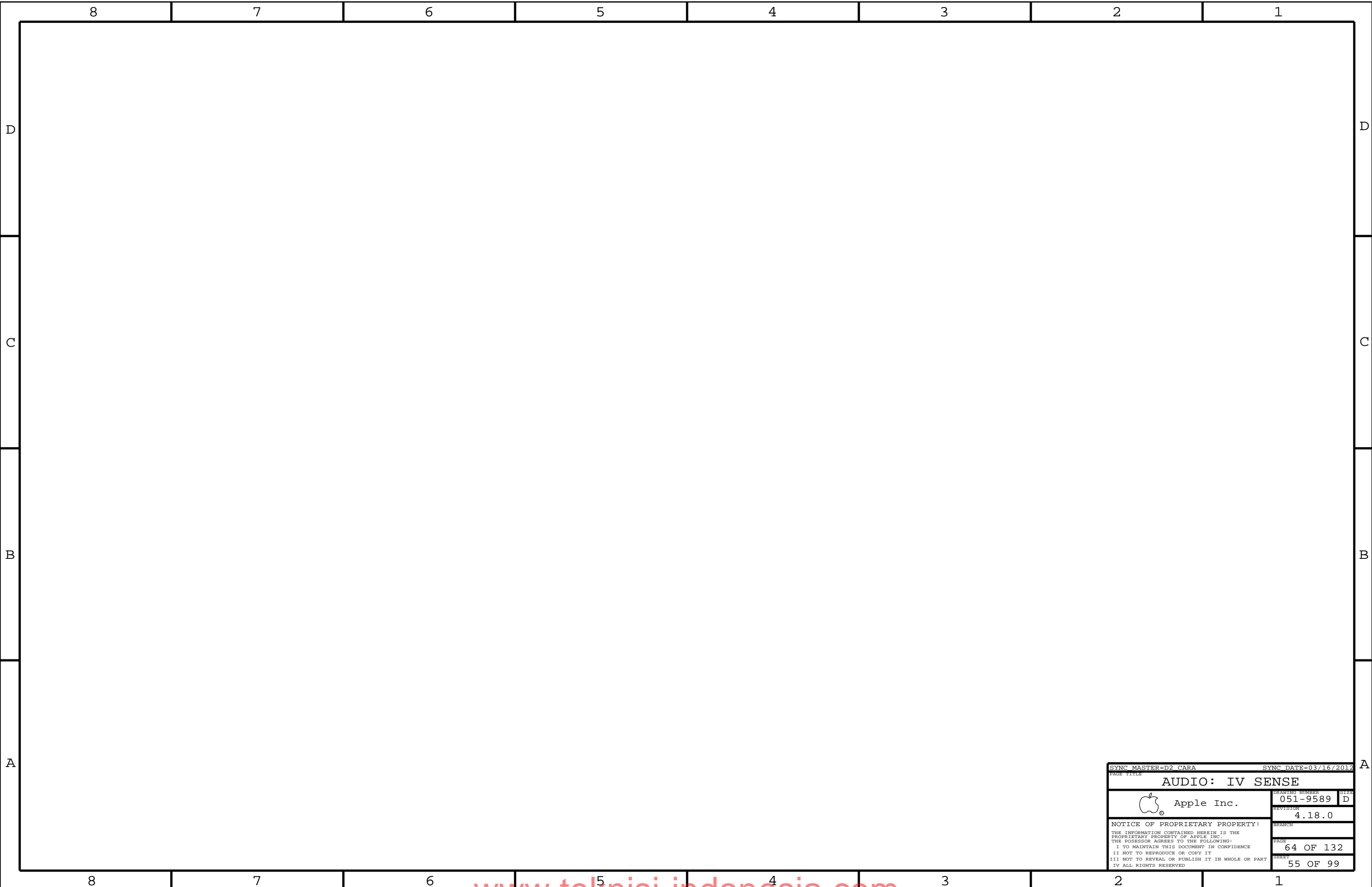
4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456

NOTES ON CODEC I/O
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

PAGE TITLE		SYNC DATE=03/16/2012	
AUDIO: CODEC/REGULATOR		DRAWING NUMBER	051-9589
Apple Inc.		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	62 OF 132
		SHEET	53 OF 99




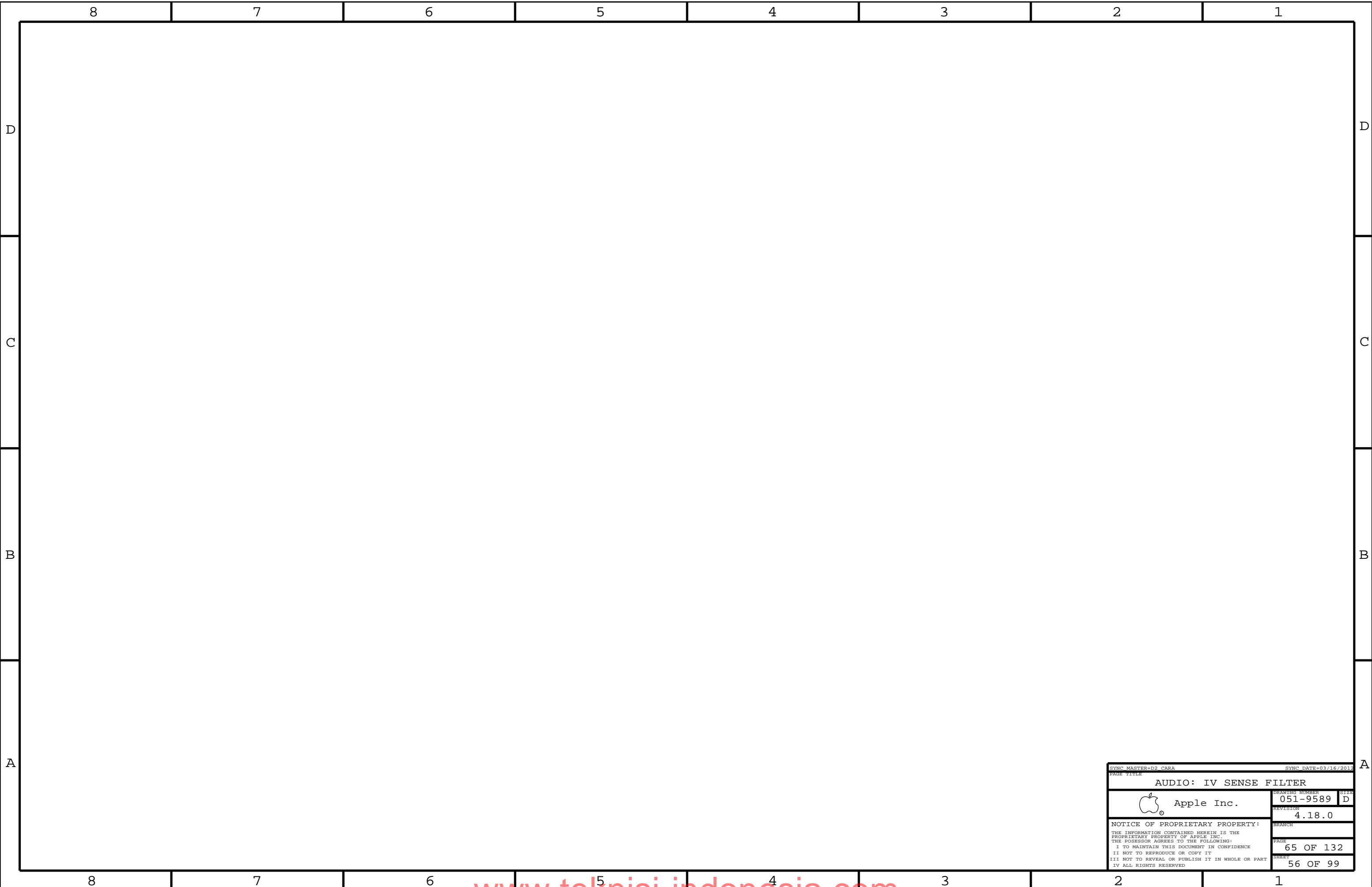
SYNC MASTER=D2 CARA		SYNC DATE=03/16/2012	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9589		D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION		4.18.0
	BRANCH		
PAGE		63 OF 132	
SHEET		54 OF 99	



SYNC MASTER=D2_CARA

SYNC DATE=03/16/2012


PAGE TITLE		AUDIO: IV SENSE	
 Apple Inc.		DRAWING NUMBER	051-9589
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	64 OF 132
		SHEET	55 OF 99



SYNC MASTER=D2 CARA

SYNC DATE=03/16/2012

AUDIO: IV SENSE FILTER

 Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER
051-9589

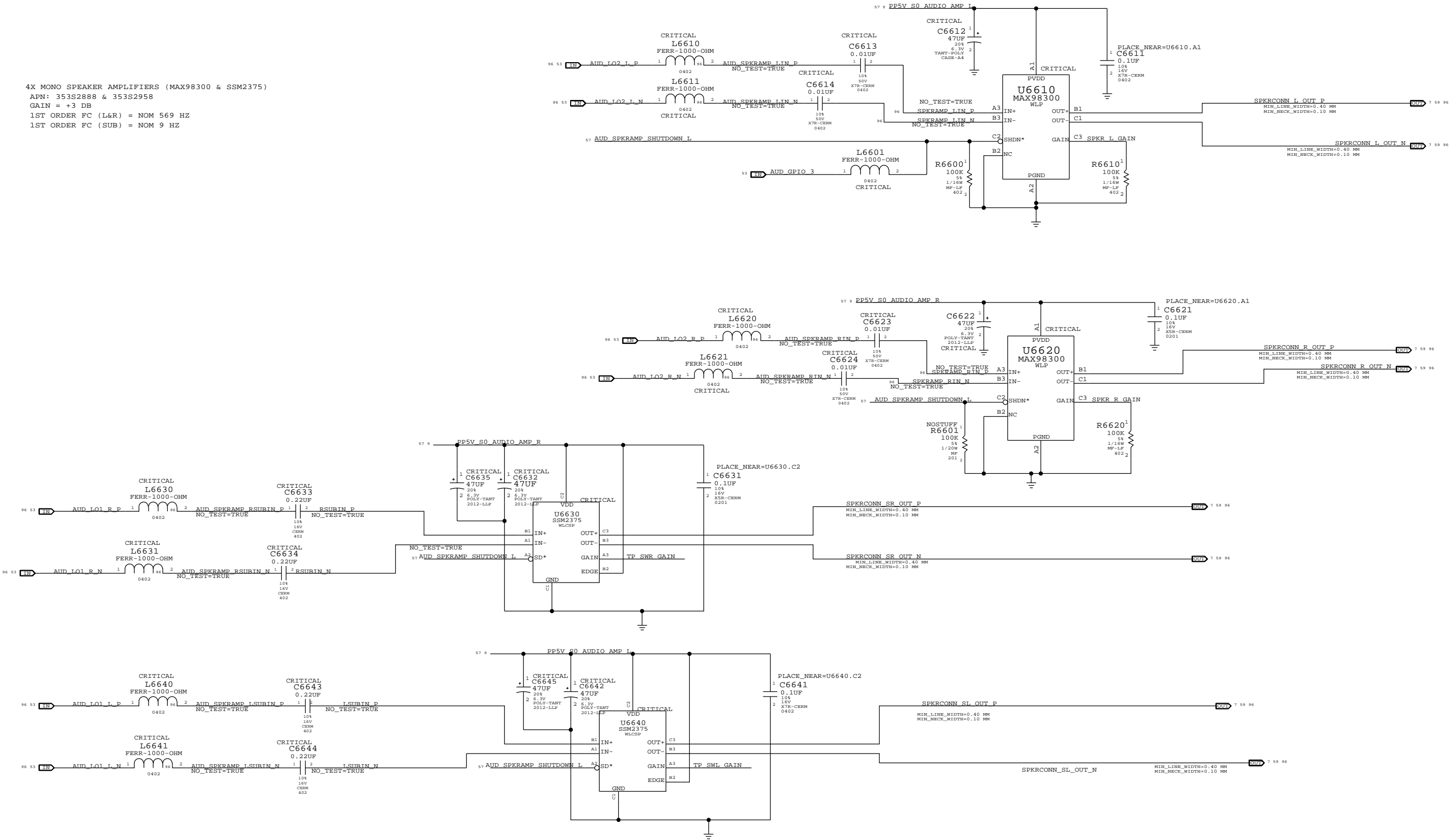
REVISION
4.18.0


BRANCH

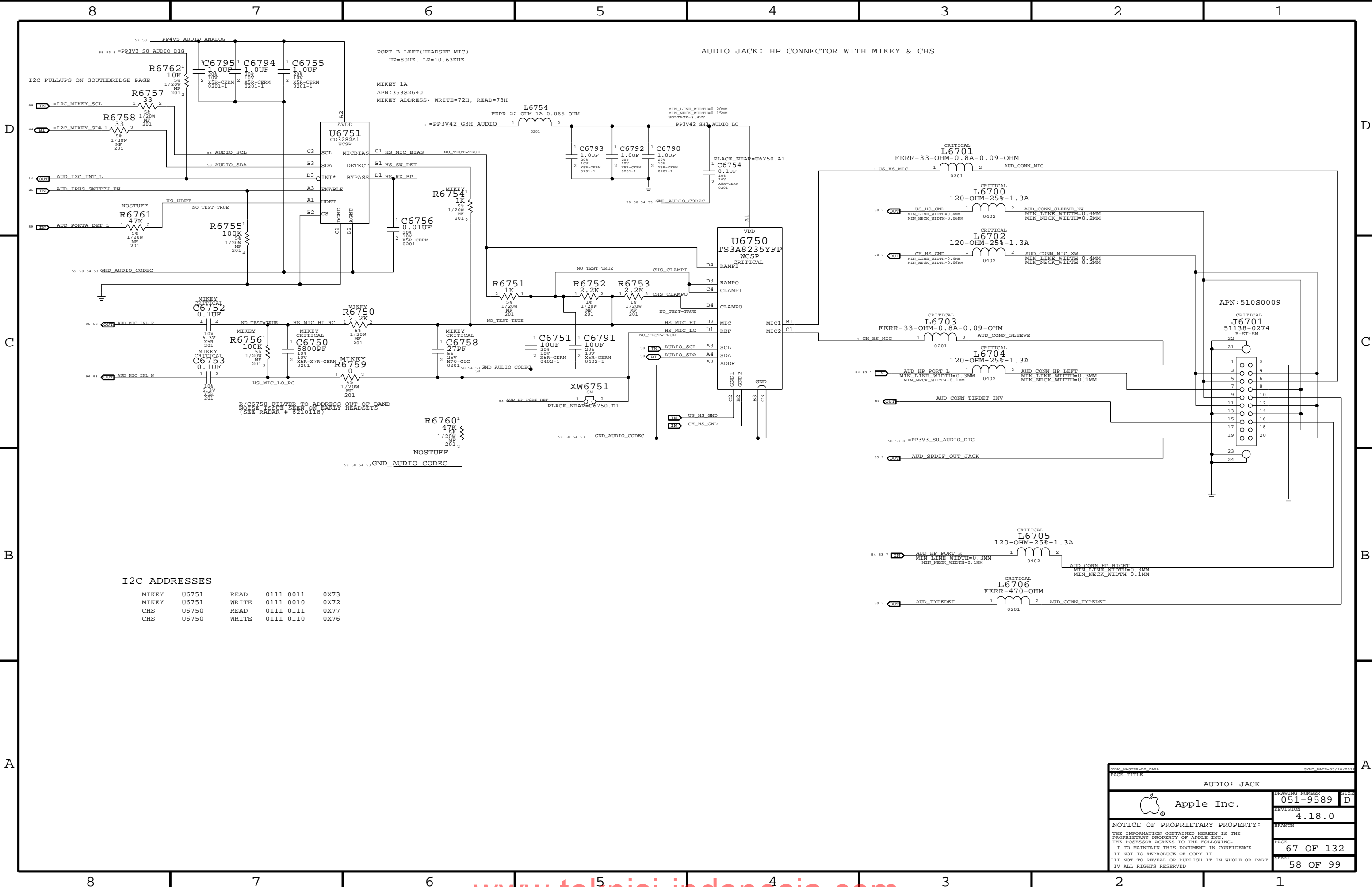
PAGE
65 OF 132

SHEET
56 OF 99

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=D2 CARA		SYNC DATE=03/16/2012	
PAGE TITLE			
AUDIO: SPEAKER AMP			
 Apple Inc.		DRAWING NUMBER	051-9589
		SIZE	D
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	66 OF 132
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	57 OF 99
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			




I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC: PARTNER-002_CARA

SYNC: DATE=03/16/2015

AUDIO: JACK

 Apple Inc.

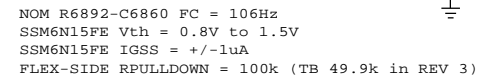
051-9589

4.18.0


NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

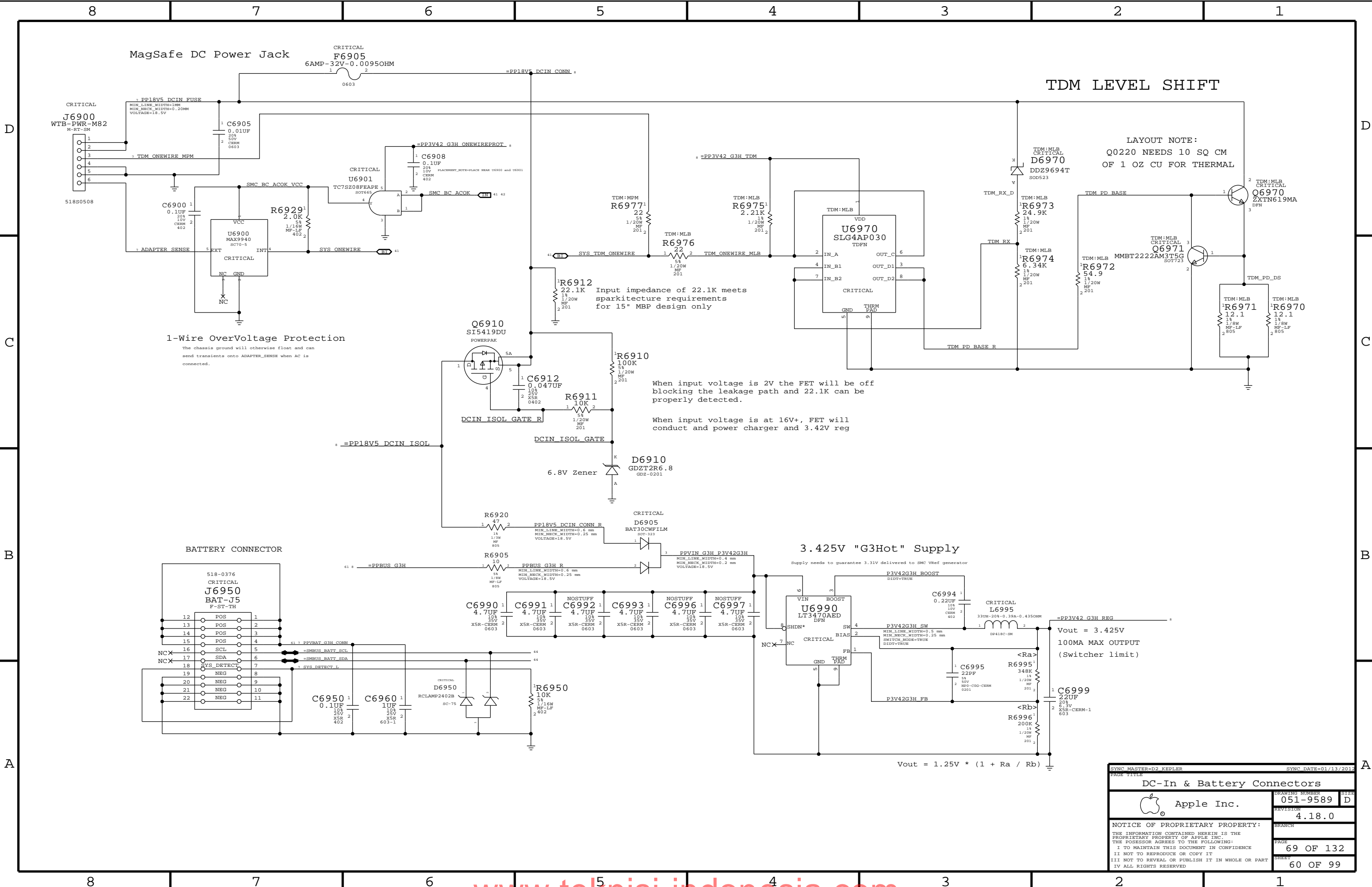
67 OF 132


58 OF 99

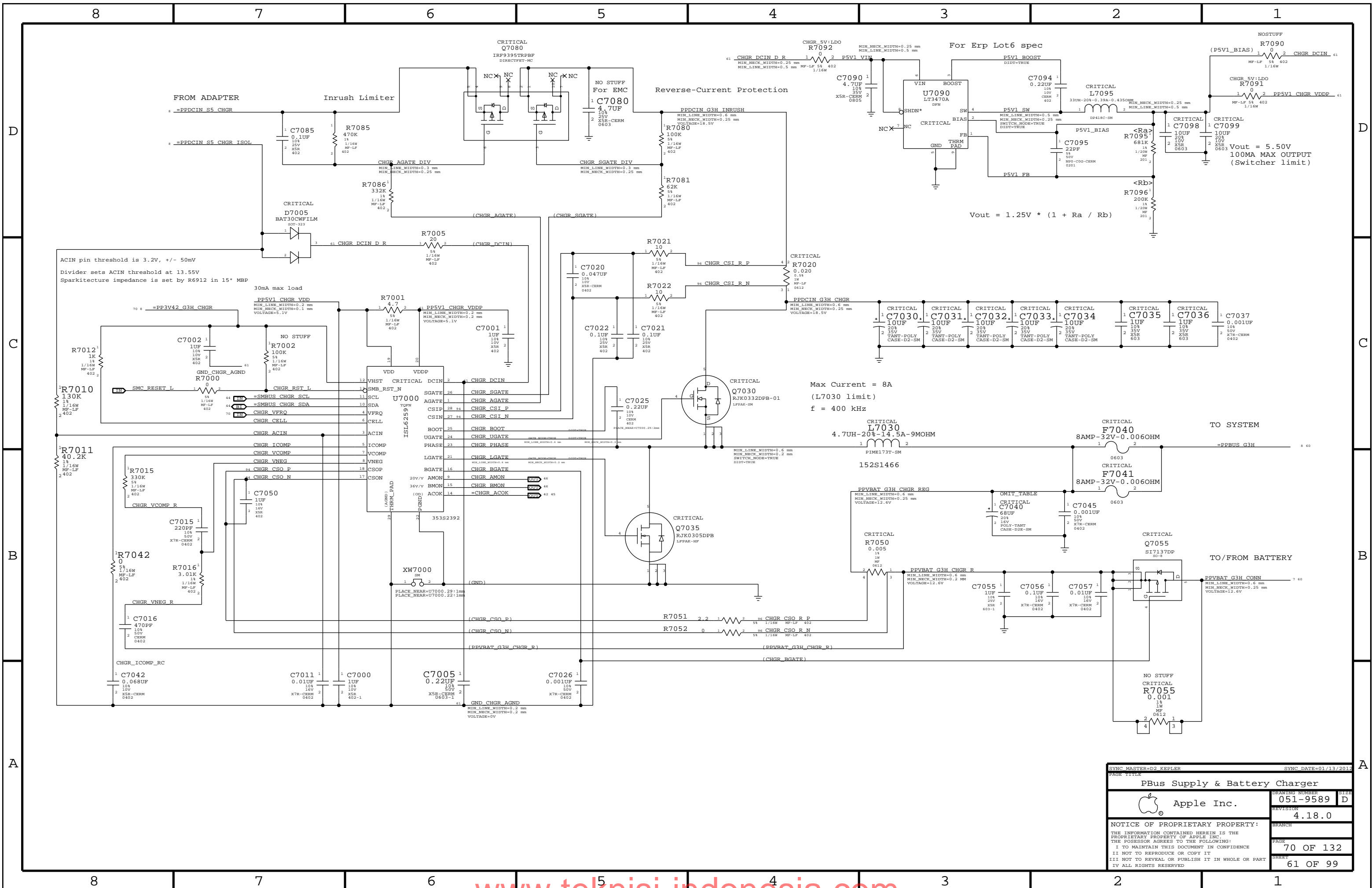


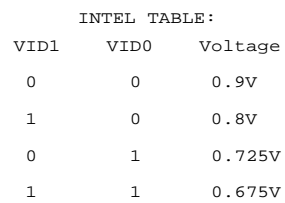
AUDIO CONNECTOR DETECT STATES			
	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYDEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

SYNC MASTER=D2 CARA		SYNC DATE=03/16/2013	
PAGE TITLE			
AUDIO: JACK TRANSLATORS			
	DRAWING NUMBER		SIZE
	051-9589		D
	REVISION		
Apple Inc.		4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE			
PROPRIETARY PROPERTY OF APPLE INC.			
THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		68 OF 132	
I NOT TO REPRODUCE OR COPY IT			
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET	
ALL RIGHTS RESERVED		59 OF 99	



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
DC-In & Battery Connectors			
 Apple Inc.		DRAWING NUMBER	051-9589
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	69 OF 132
		SHEET	60 OF 99



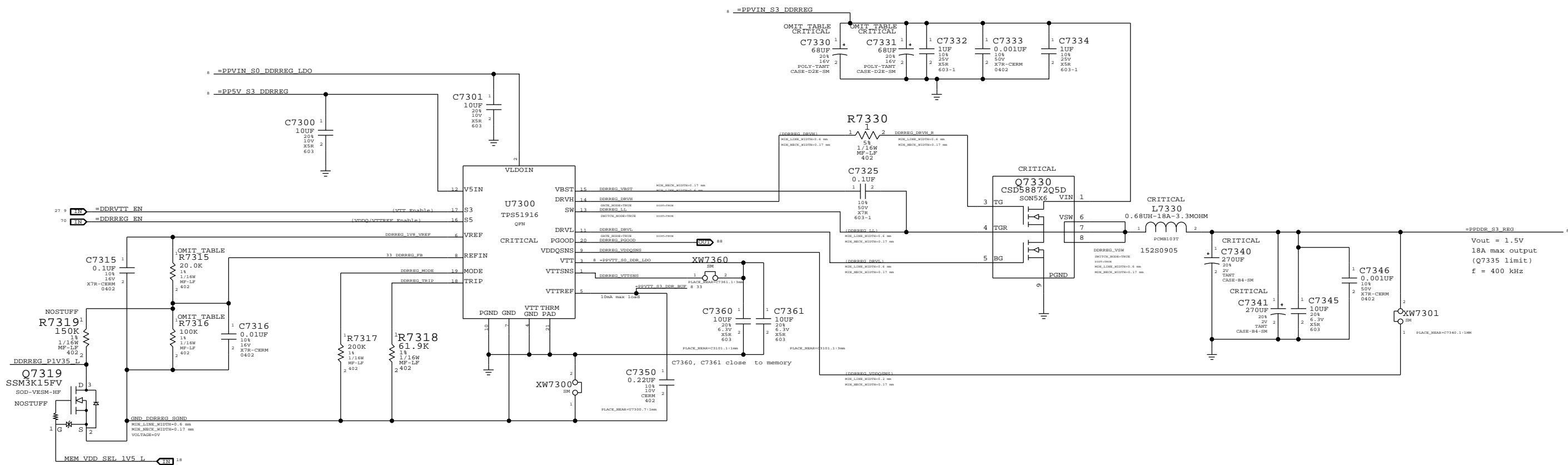


```
fb = (R7151+R7152)/R7152 = 1.349 and Vref = 0.5;
VID1=1, VIC0=1:
Vout<1,1> = Vref x fb;
VID1=0, VID0=1:
Vout<0,1> = Vref x (1+R7147 / (R7148 + R7149 )) x fb
VID1=1, VID0=0
Vout<1,0> = Vref x (1+ (R7147 + R7148) / R7149 )) x fb
VID1=0, VID0=0
Vout<0,0> = Vref x (1+ (R7147 / (R7148 + R7149 // R7150 )) x fb
```

$$\begin{aligned} \text{OCP} &= R_{7141} \times 8.5\mu\text{A} / R_{7140} \\ \text{OCP} &= 8.5\text{A} \end{aligned}$$

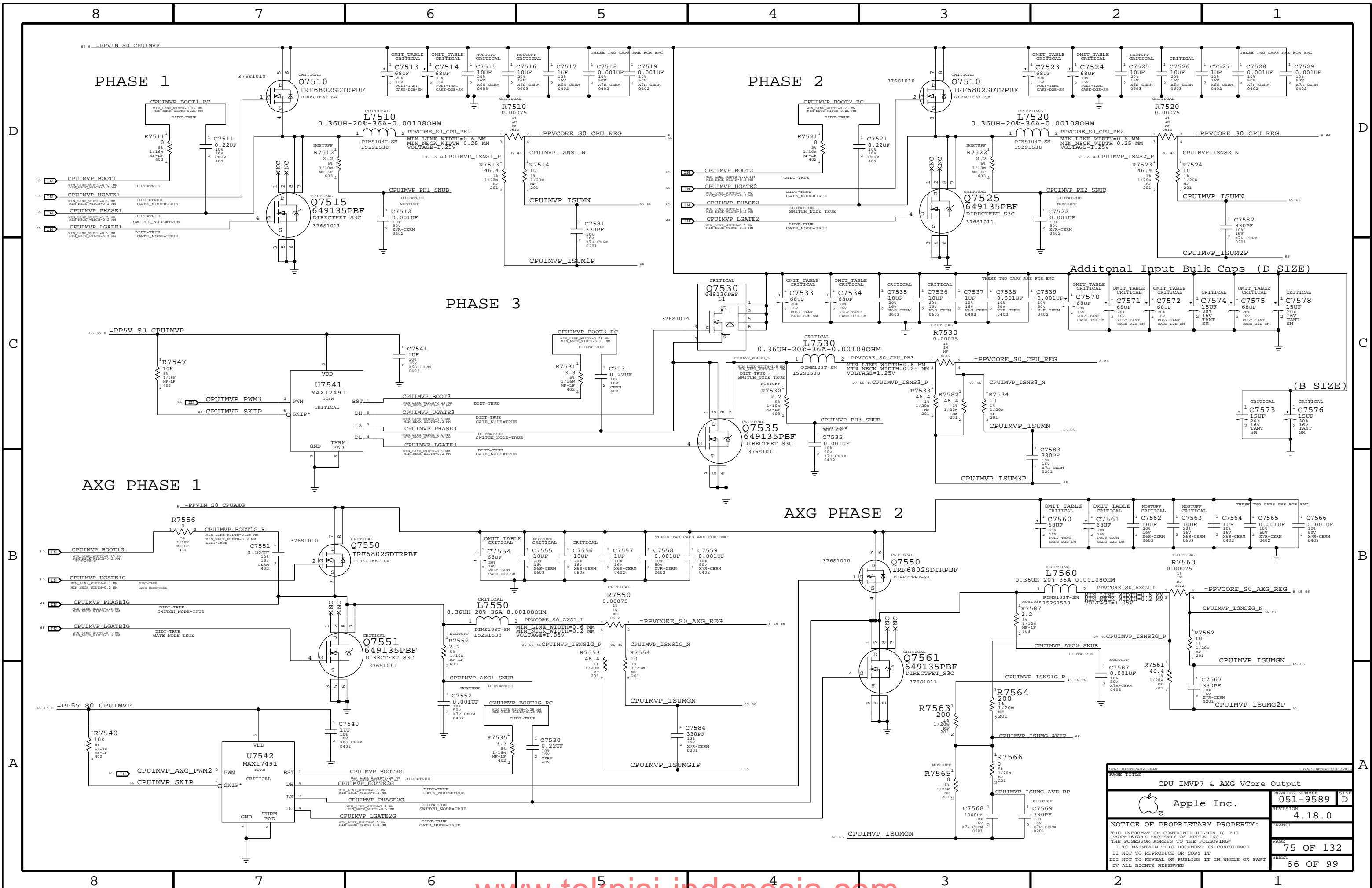


DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0343	1	RES,MTL,PT10,1/5W,20.0K,1,0402,080,LP	R7315		PPDDR:1V5
114S0342	1	RES,MTL,PT10,1/5W,19.6K,1,0402,080,LP	R7315		PPDDR:1V35
114S0411	1	RES,MTL,PT10,1/5W,100K,1,0402,080,LP	R7316		PPDDR:1V5
114S0389	1	RES,MTL,PT10,1/5W,61.9K,1,0402,080,LP	R7316		PPDDR:1V35

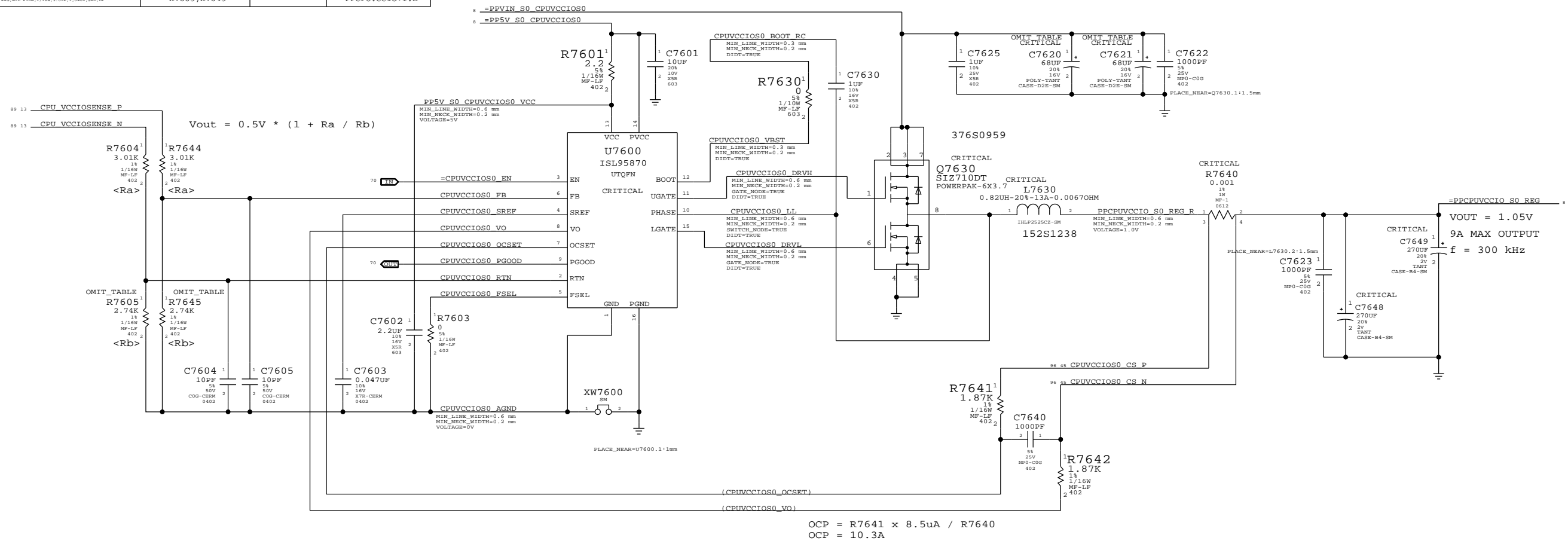
DRAWING NUMBER		051-9589	SIZE	D
REVISION		4.18.0		
BRANCH				
PAGE		73 OF 132		
SHEET		64 OF 99		




SYMC PARTSHEET: CPU IMVP7 & AXG VCore Output		SYMC DATE: 03/05/2015
PAGE TITLE		DRAWING NUMBER
Apple Inc.		051-9589
REVISION		4.18.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH
		PAGE
		75 OF 132
		SHEET
		66 OF 99

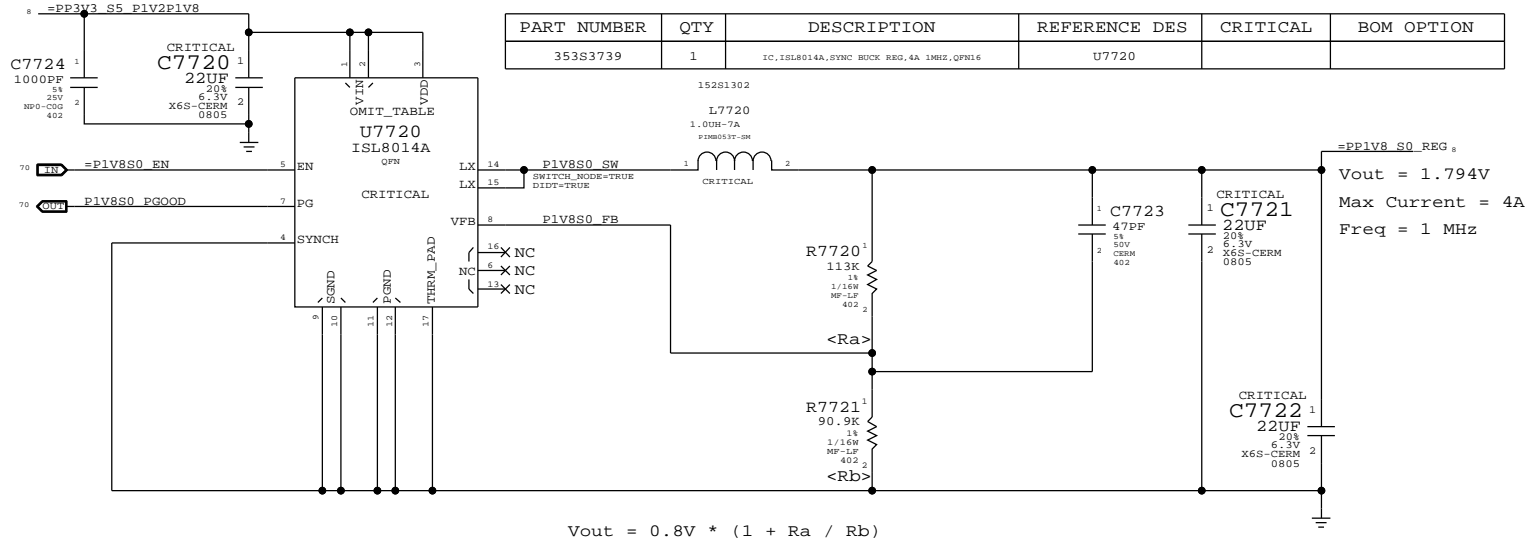
CPU VCCIO (1V0R1V05 S0) REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0260	2	REG.MTU.P10M,1/16W,2.74K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:SNB
114S0264	2	REG.MTU.P10M,1/16W,3.01K,1,0402,SMD,LF	R7605,R7645		PPCPUVCCIO:IVB



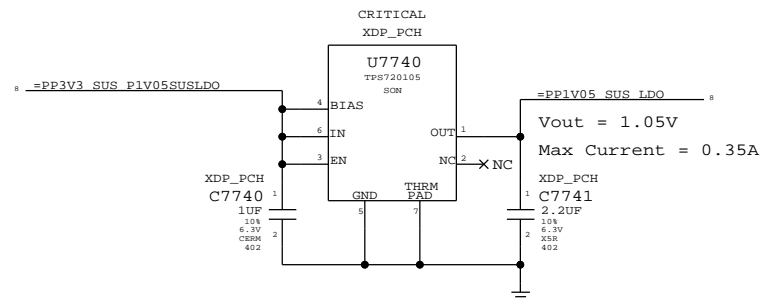
SYMC MASTER-D2 KEPLER		SYMC DATE=01/13/2015	
PAGE TITLE			
CPU VCCIO (1V0R1V05 S0) POWER SUPPLY			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE D
	REVISION	4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	76 OF 132
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	67 OF 99
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

1.8V S0 Regulator

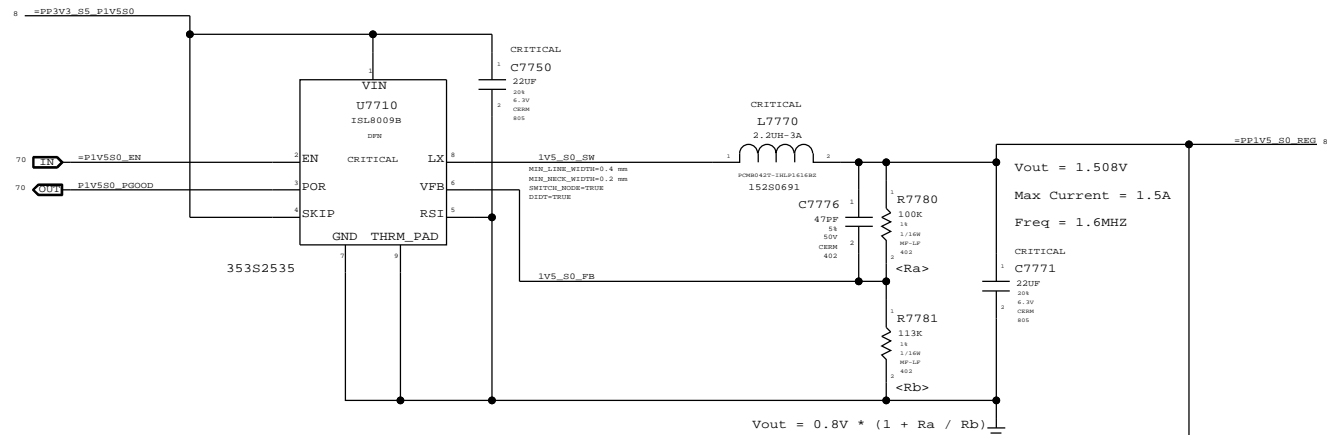


1.05V SUS LDO

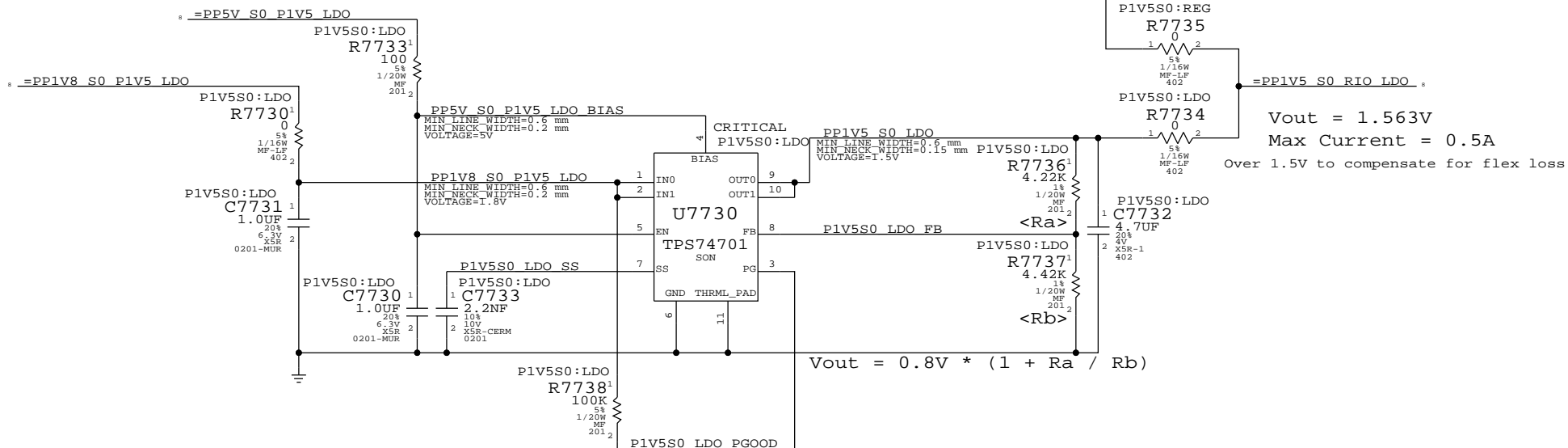
Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.




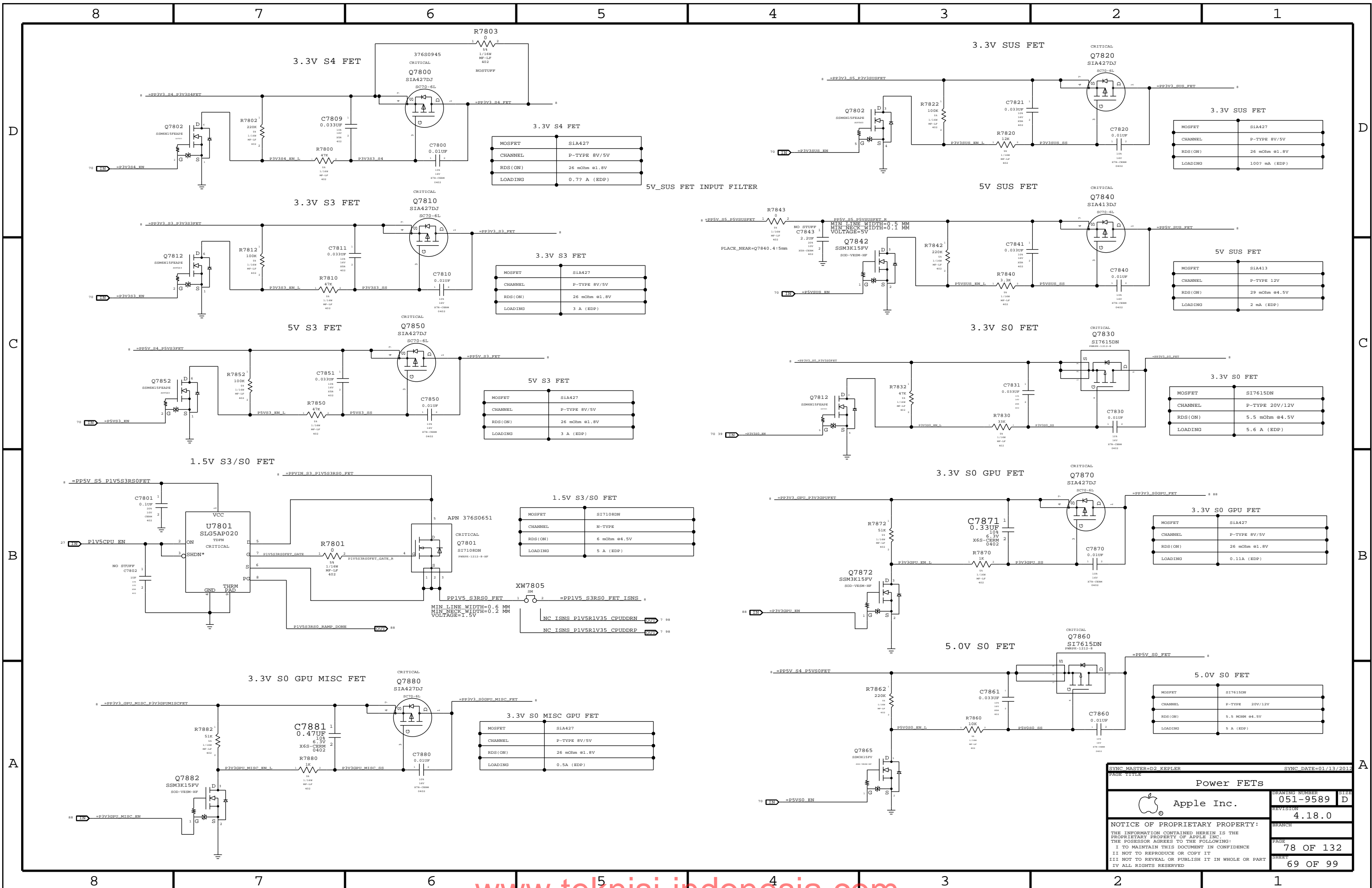
1.5V S0 Regulator



1.5V S0 LDO (RIO)



SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
Misc Power Supplies			
	Apple Inc.	DRAWING NUMBER	051-9589
		SIZE	D
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	77 OF 132
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	68 OF 99
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



D

C

B

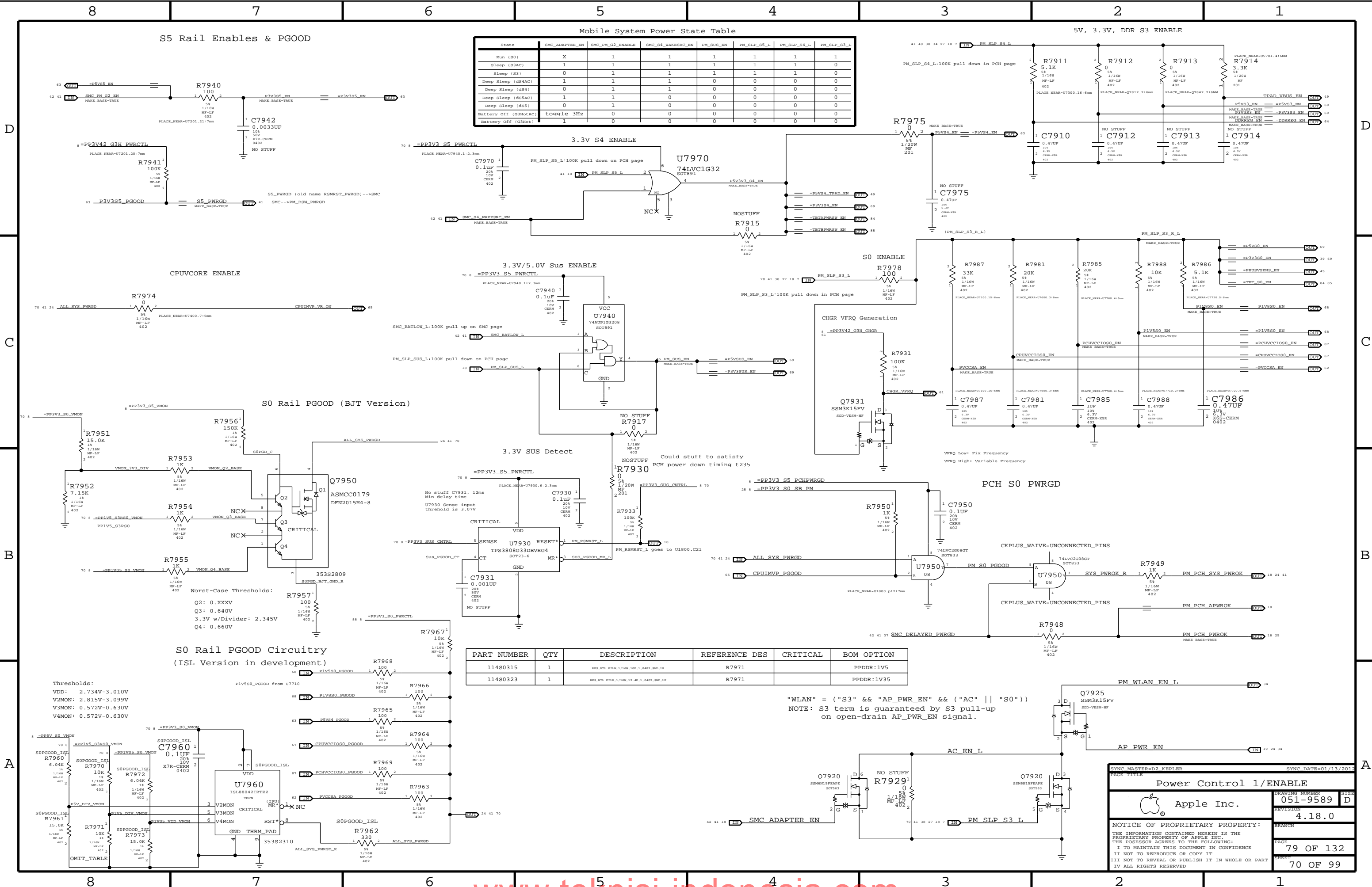
A

D

C

B

A



Mobile System Power State Table							
State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_MAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Deep Sleep (dS4AC)	0	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0315	1	RES,MTL,F10M,1/16W,10K,1,0402,080,LP	R7971		PPDDR:1V5
114S0323	1	RES,MTL,F10M,1/16W,12.4K,1,0402,080,LP	R7971		PPDDR:1V35

SYNC MASTER=D2 KEPLER

PAGE TITLE

Power Control 1/ENABLE

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

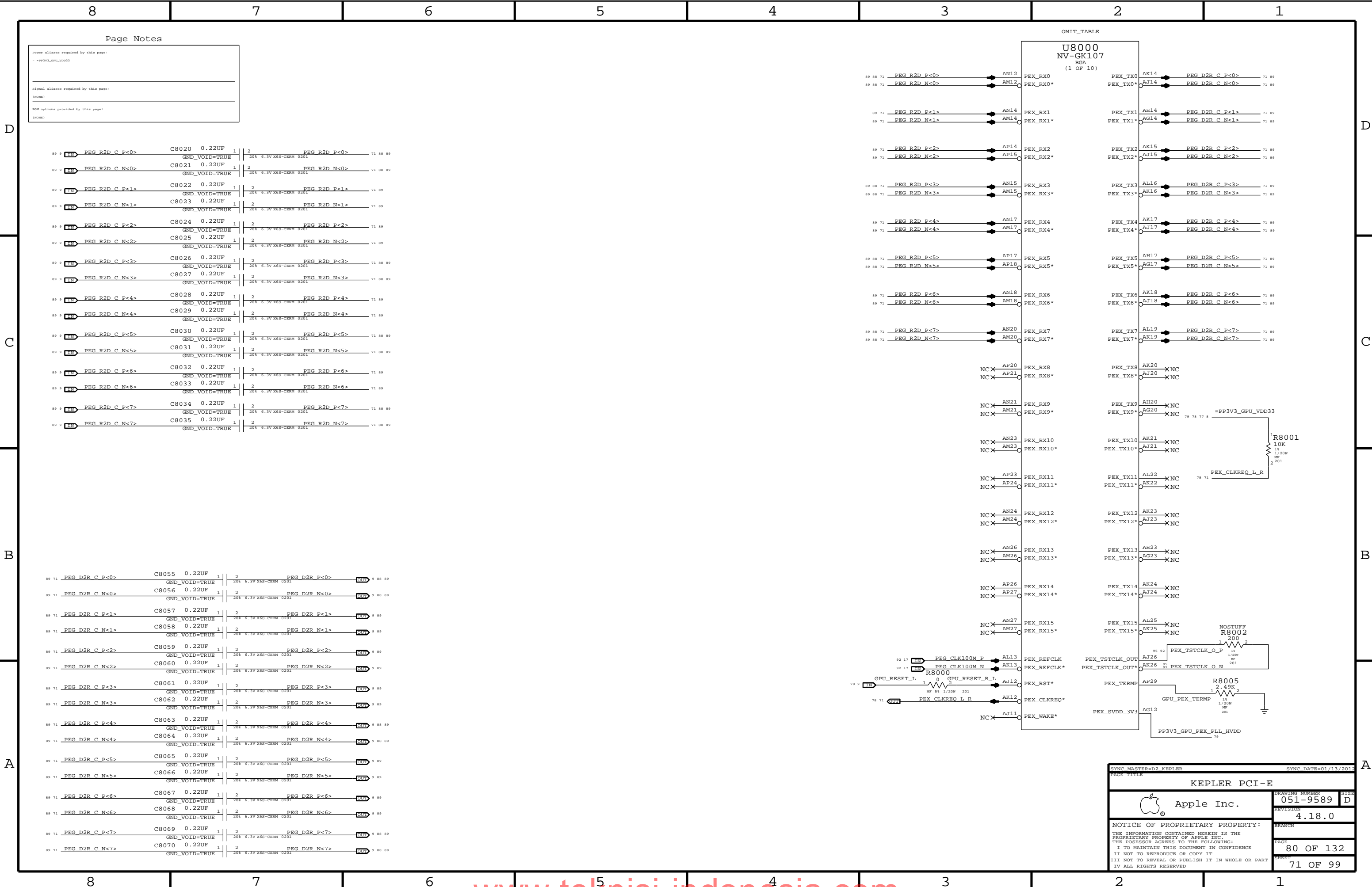
SYNC DATE=01/13/2012

DRAWING NUMBER
051-9589

REVISION
4.18.0

PAGE
79 OF 132

SHEET
70 OF 99



Page Notes

Power aliases required by this page:
--PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

89 9	PEG R2D C P<0>	C8020	0.22UF	1	2	PEG R2D P<0>	71 88 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<0>	C8021	0.22UF	1	2	PEG R2D N<0>	71 88 89
			GND_VOID=TRUE				
89 9	PEG R2D C P<1>	C8022	0.22UF	1	2	PEG R2D P<1>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<1>	C8023	0.22UF	1	2	PEG R2D N<1>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C P<2>	C8024	0.22UF	1	2	PEG R2D P<2>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<2>	C8025	0.22UF	1	2	PEG R2D N<2>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C P<3>	C8026	0.22UF	1	2	PEG R2D P<3>	71 88 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<3>	C8027	0.22UF	1	2	PEG R2D N<3>	71 88 89
			GND_VOID=TRUE				
89 9	PEG R2D C P<4>	C8028	0.22UF	1	2	PEG R2D P<4>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<4>	C8029	0.22UF	1	2	PEG R2D N<4>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C P<5>	C8030	0.22UF	1	2	PEG R2D P<5>	71 88 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<5>	C8031	0.22UF	1	2	PEG R2D N<5>	71 88 89
			GND_VOID=TRUE				
89 9	PEG R2D C P<6>	C8032	0.22UF	1	2	PEG R2D P<6>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<6>	C8033	0.22UF	1	2	PEG R2D N<6>	71 89
			GND_VOID=TRUE				
89 9	PEG R2D C P<7>	C8034	0.22UF	1	2	PEG R2D P<7>	71 88 89
			GND_VOID=TRUE				
89 9	PEG R2D C N<7>	C8035	0.22UF	1	2	PEG R2D N<7>	71 88 89
			GND_VOID=TRUE				

89 71	PEG D2R C P<0>	C8055	0.22UF	1	2	PEG D2R P<0>	9 88 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<0>	C8056	0.22UF	1	2	PEG D2R N<0>	9 88 89
			GND_VOID=TRUE				
89 71	PEG D2R C P<1>	C8057	0.22UF	1	2	PEG D2R P<1>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<1>	C8058	0.22UF	1	2	PEG D2R N<1>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C P<2>	C8059	0.22UF	1	2	PEG D2R P<2>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<2>	C8060	0.22UF	1	2	PEG D2R N<2>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C P<3>	C8061	0.22UF	1	2	PEG D2R P<3>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<3>	C8062	0.22UF	1	2	PEG D2R N<3>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C P<4>	C8063	0.22UF	1	2	PEG D2R P<4>	9 88 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<4>	C8064	0.22UF	1	2	PEG D2R N<4>	9 88 89
			GND_VOID=TRUE				
89 71	PEG D2R C P<5>	C8065	0.22UF	1	2	PEG D2R P<5>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<5>	C8066	0.22UF	1	2	PEG D2R N<5>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C P<6>	C8067	0.22UF	1	2	PEG D2R P<6>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<6>	C8068	0.22UF	1	2	PEG D2R N<6>	9 89
			GND_VOID=TRUE				
89 71	PEG D2R C P<7>	C8069	0.22UF	1	2	PEG D2R P<7>	9 88 89
			GND_VOID=TRUE				
89 71	PEG D2R C N<7>	C8070	0.22UF	1	2	PEG D2R N<7>	9 88 89
			GND_VOID=TRUE				

SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

KEPLER PCI-E

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

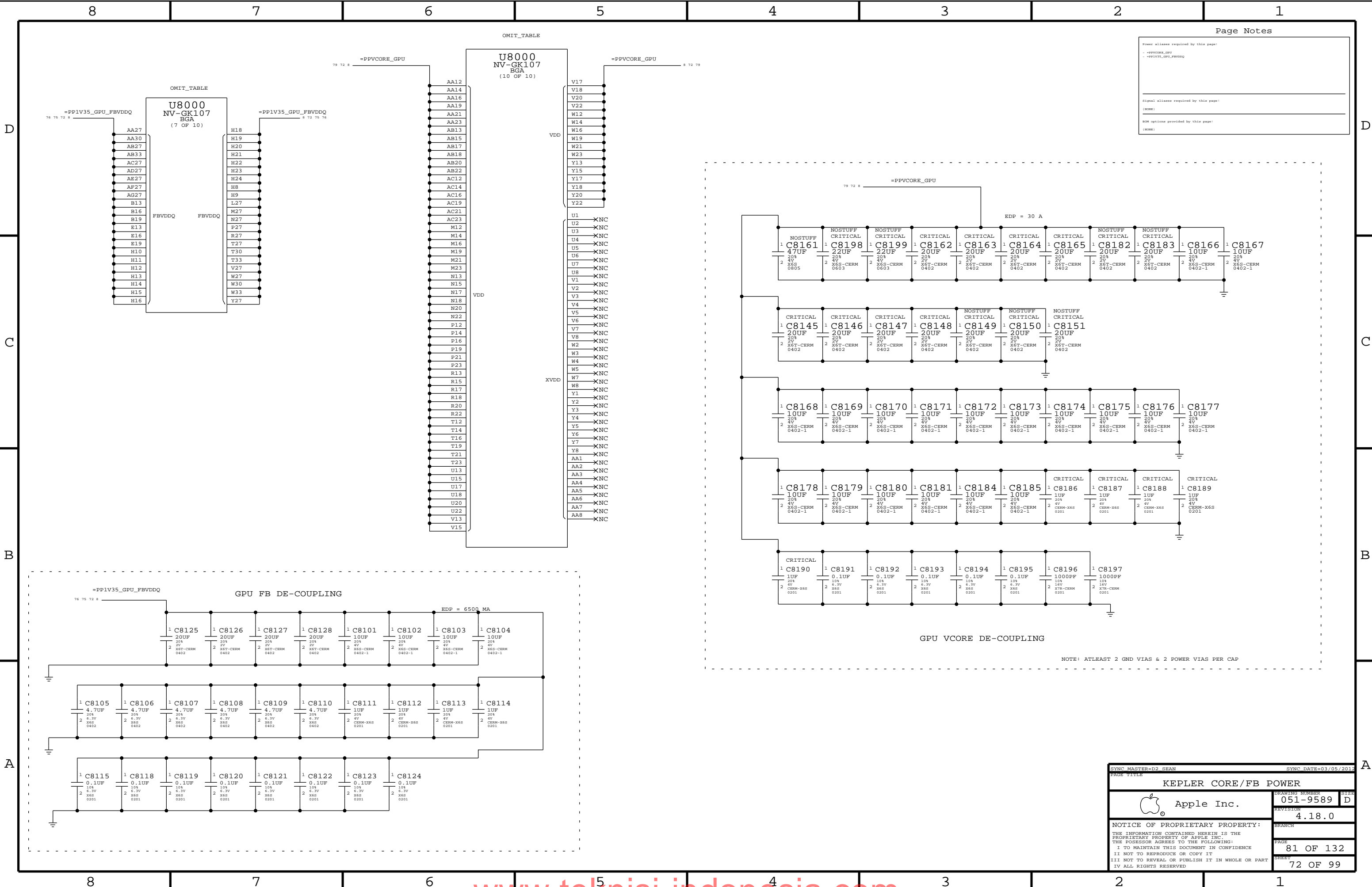
DRAWING NUMBER
051-9589

REVISION
4.18.0


BRANCH

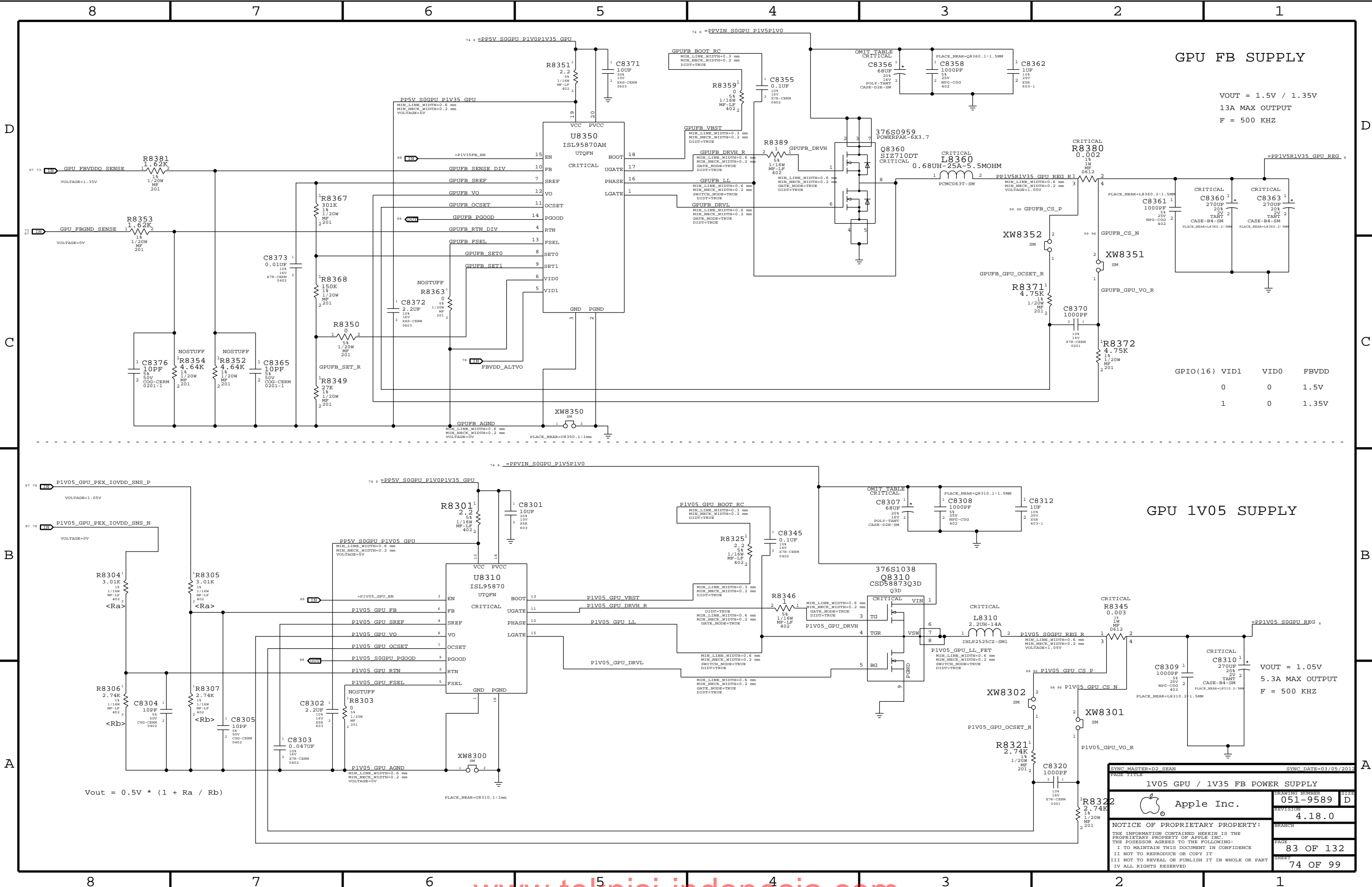
PAGE
80 OF 132

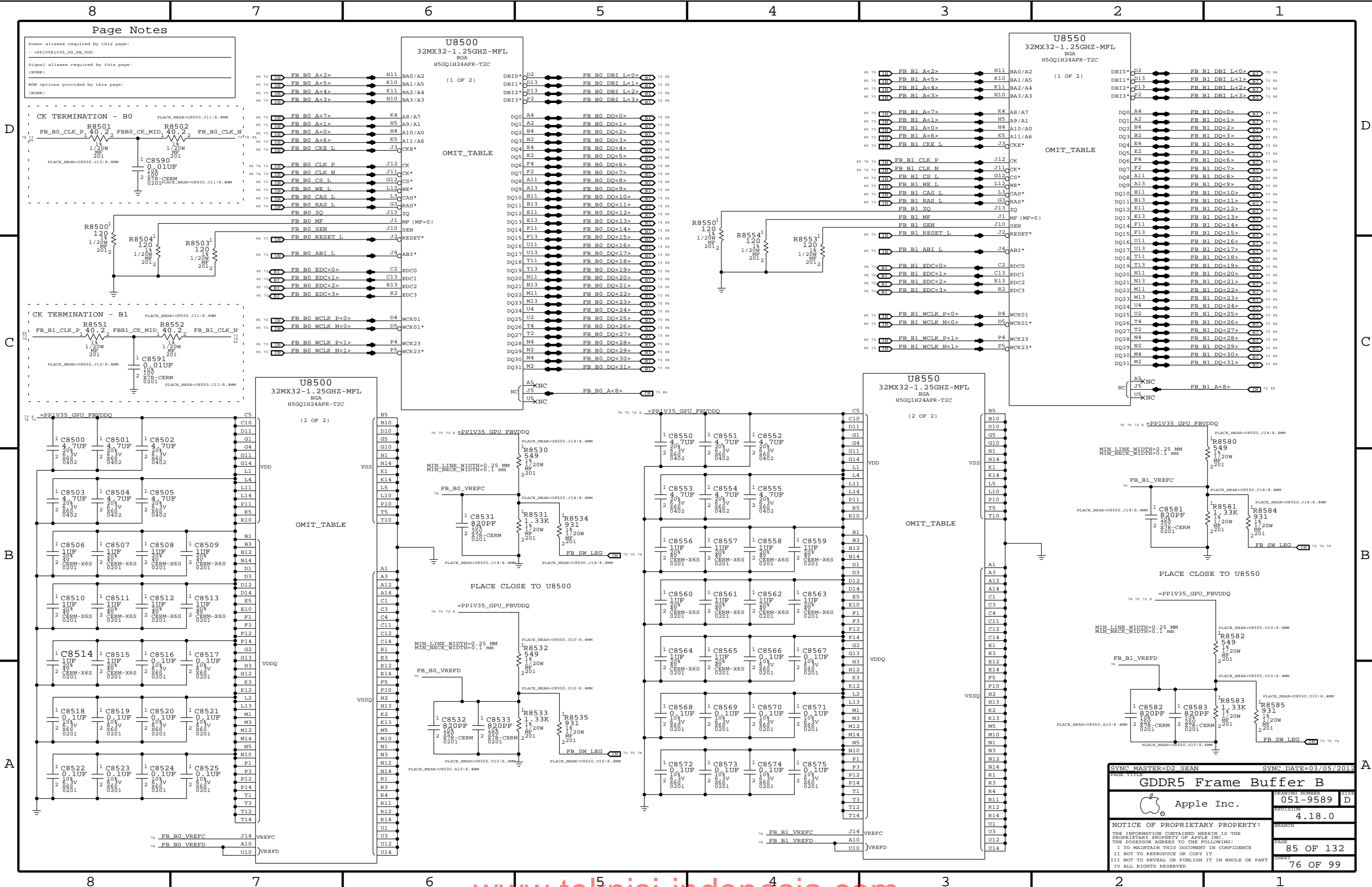
SHEET
71 OF 99



Page Notes	
Power aliases required by this page:	
- =PPVCORE_GPU	
- =PPV35_GPU_FBVDDQ	
Signal aliases required by this page:	
(NONE)	
BOM options provided by this page:	
(NONE)	

SYNC MASTER=D2 SEAN		SYNC DATE=03/05/2012	
PAGE TITLE			
KEPLER CORE/FB POWER		DRAWING NUMBER	
 Apple Inc.	051-9589		SIZE
	REVISION		D
		4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		81 OF 132	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		72 OF 99	
IV ALL RIGHTS RESERVED			



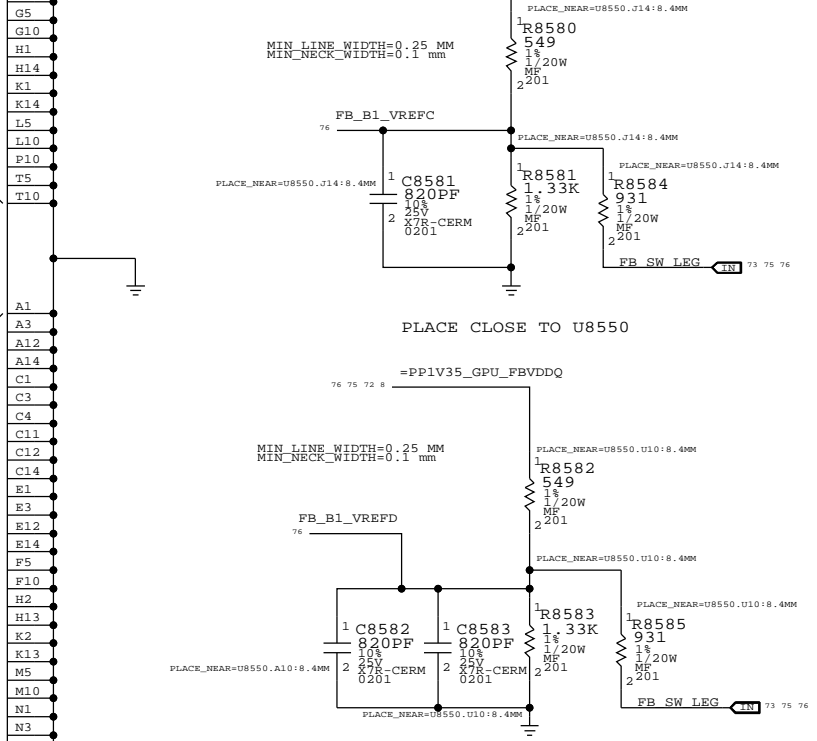
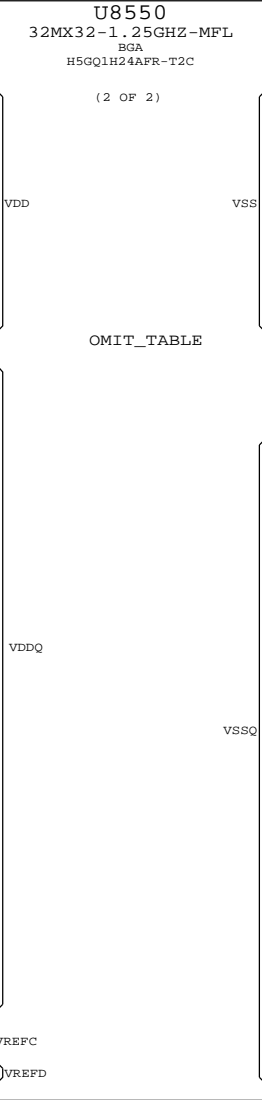
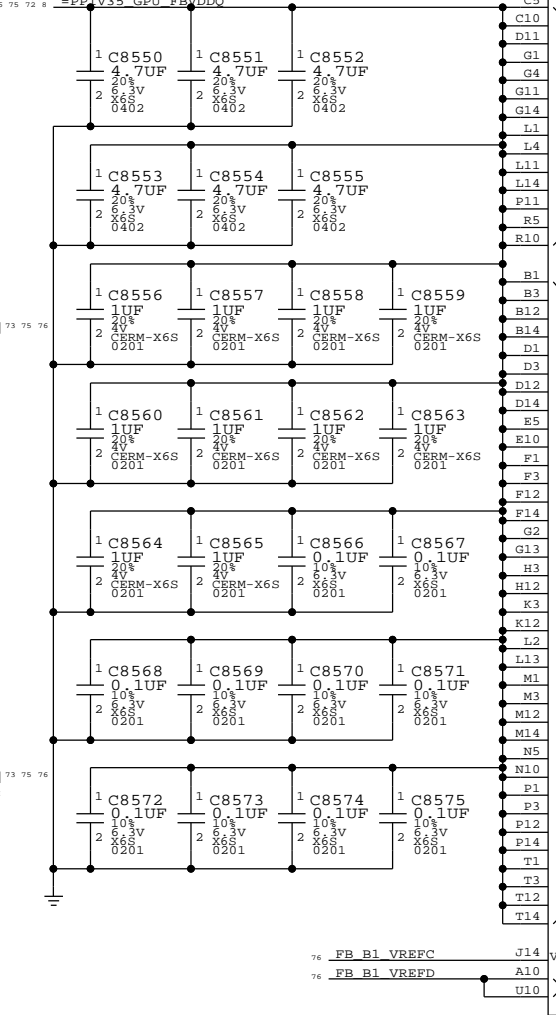
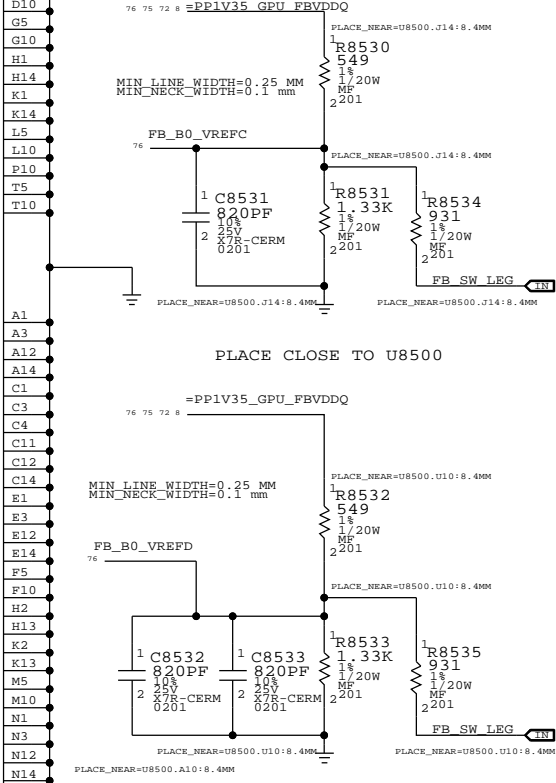
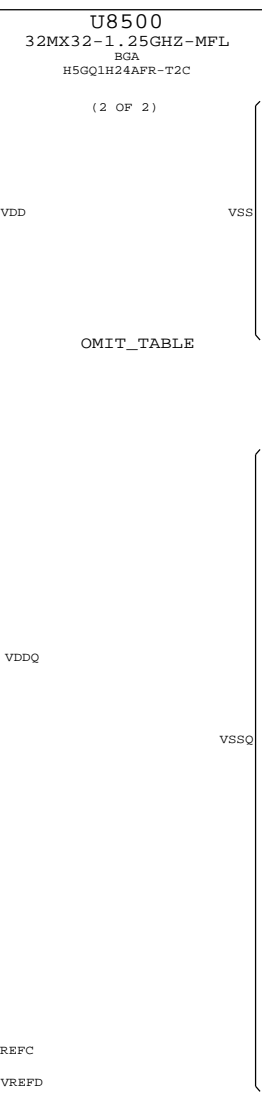
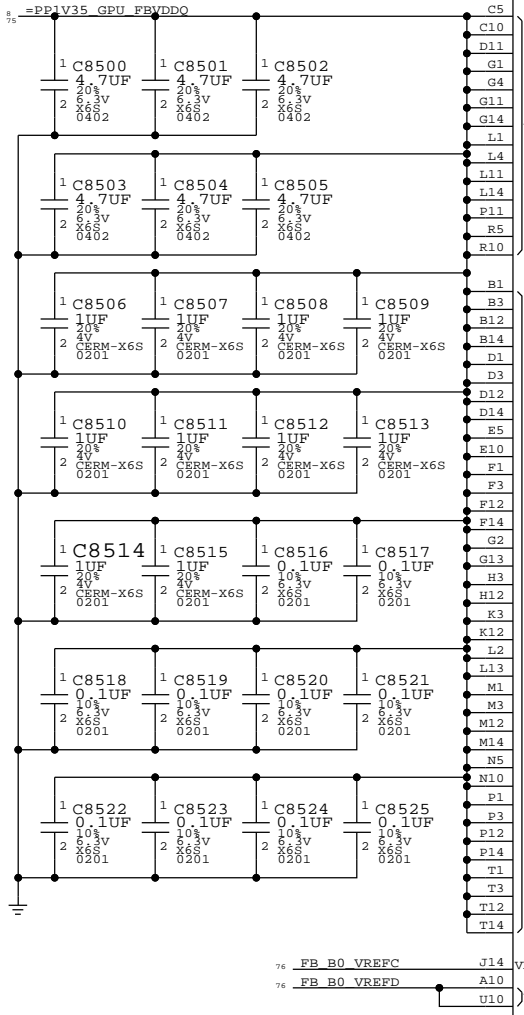
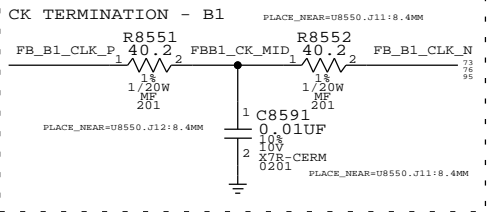
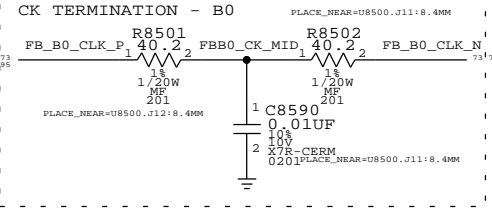



Page Notes

Power aliases required by this page:
- =PP1V35 GPU_FB_VDD

Signal aliases required by this page:
(NONE)

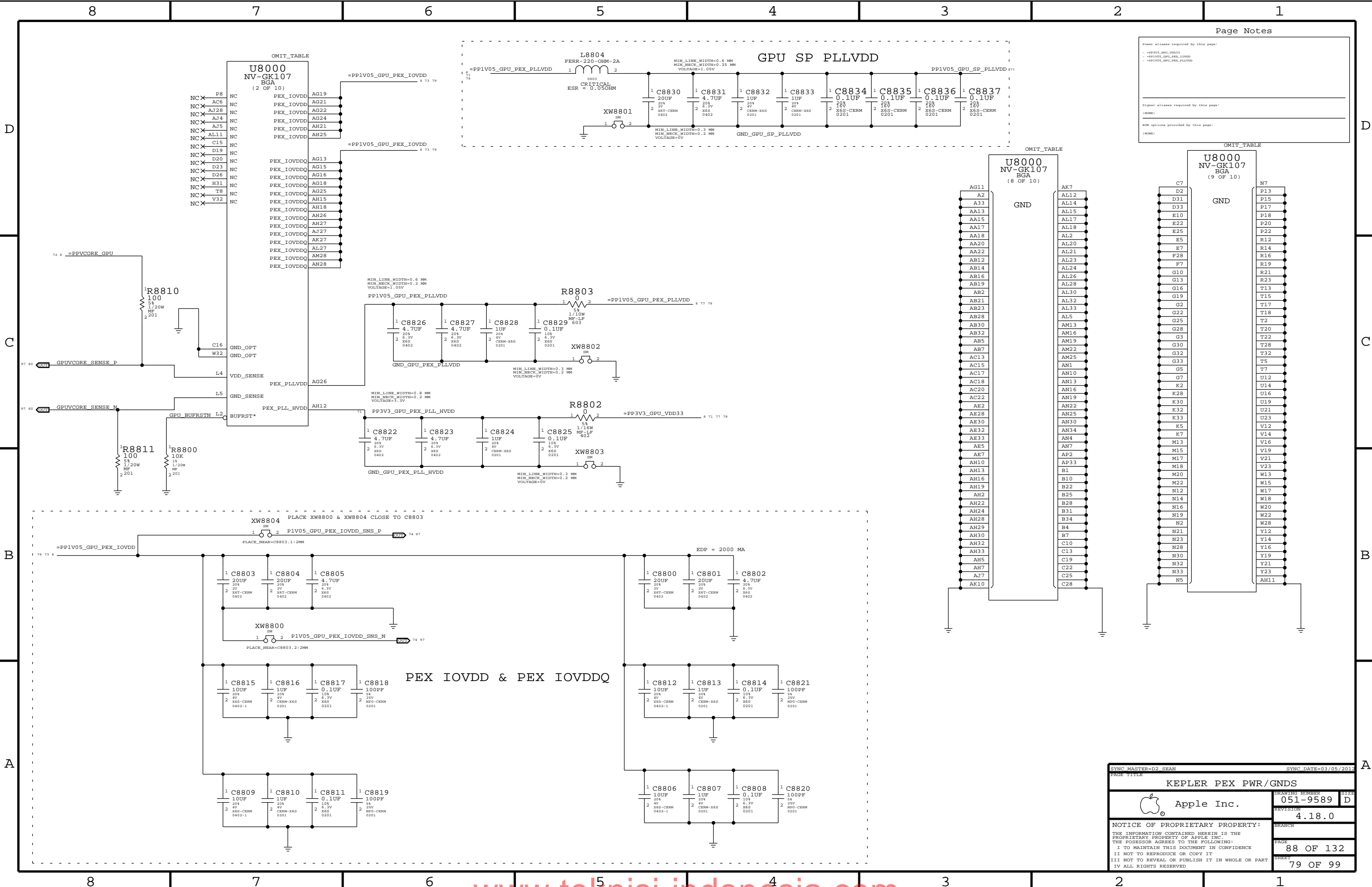
BOM options provided by this page:
(NONE)



SYNC MASTER=D2 SEAN		SYNC DATE=03/05/2012	
PAGE TITLE			
GDDR5 Frame Buffer B			
	DRAWING NUMBER		SIZE
	051-9589		D
	REVISION		
		4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		85 OF 132	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		76 OF 99	
IV ALL RIGHTS RESERVED			







Page Notes

Power aliases required by this page:


- PP3V3_GPU_VDD33
- PP1V05_GPU_PEX_IOVDD
- PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

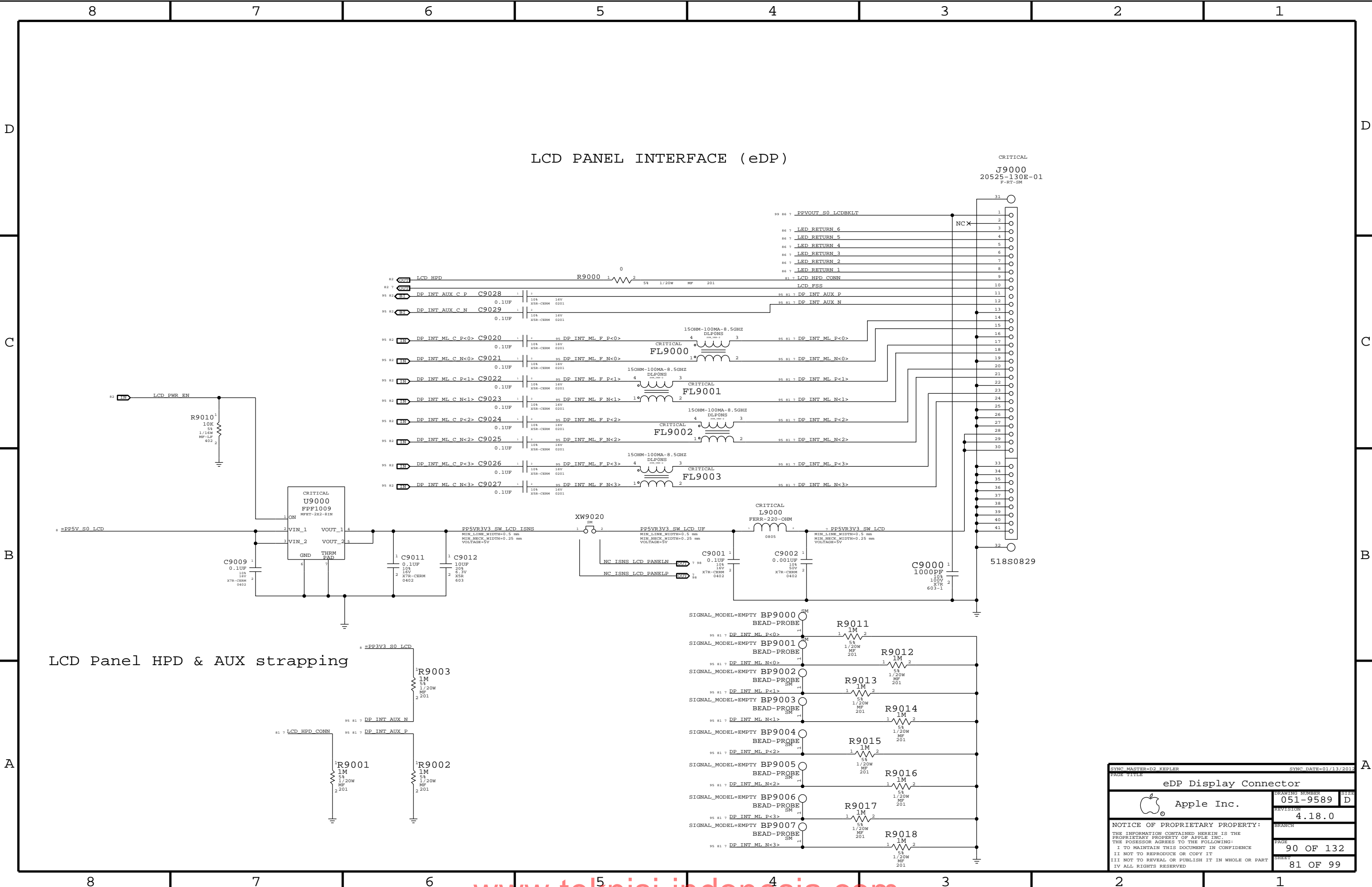
(NONE)

NOT options provided by this page:

(NONE)

SYNC MASTER=D2 SEAN		SYNC DATE=03/05/2012	
PAGE TITLE			
KEPLER PEX PWR/GNDS			
	Apple Inc.	DRAWING NUMBER	051-9589
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		PAGE 88 OF 132	
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET 79 OF 99	
IV ALL RIGHTS RESERVED			






LCD Panel HPD & AUX strapping

SYNC MASTER=D2 FEEDER

SYNC DATE=01/13/2012

PAGE TITLE

eDP Display Connector

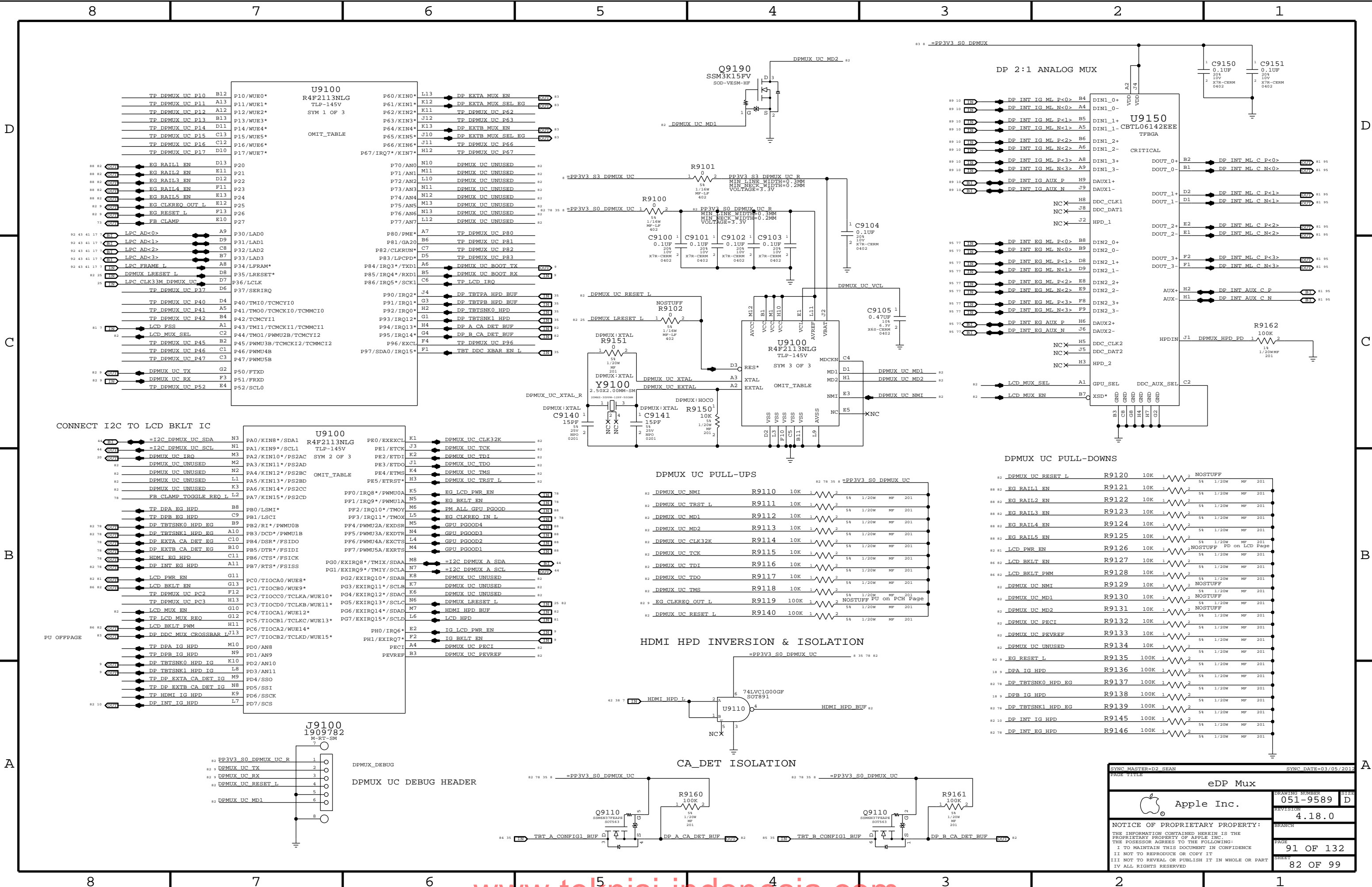
 Apple Inc.

DRAWING NUMBER
051-9589

REVISION
4.18.0

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BRANCH
PAGE
90 OF 132
SHEET
81 OF 99




SYNC MASTER=D2 SEAN

SYNC DATE=03/05/2012

PAGE TITLE

eDP Mux

 Apple Inc.

Drawing Number
051-9589

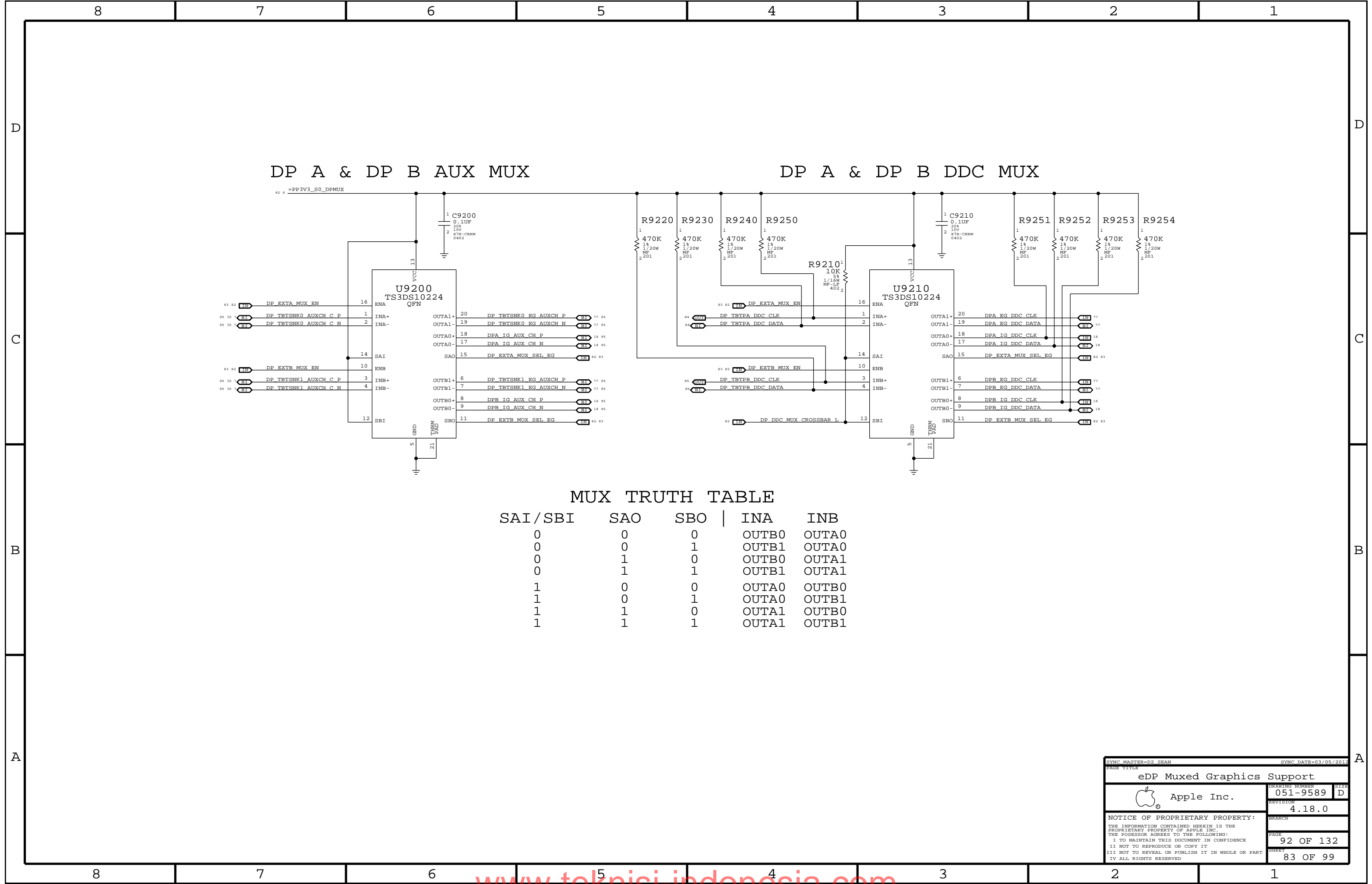
Revision
4.18.0

Branch

Page
91 OF 132

Sheet
82 OF 99

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



DP A & DP B AUX MUX

DP A & DP B DDC MUX

MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC MASTER=D2 SEAN

SYNC DATE=03/05/2012

eDP Muxed Graphics Support

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE
PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER
051-9589

REVISION
4.18.0

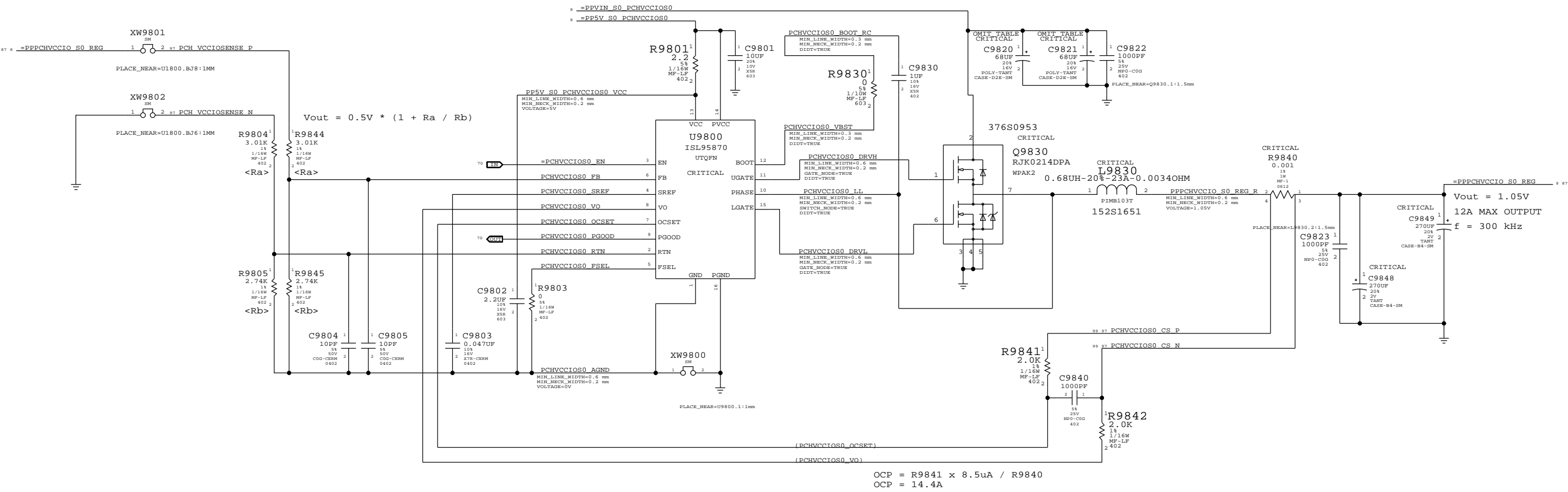
PAGE
92 OF 132

SHEET
83 OF 99

SIZE
D



PCH VCCIO (1.05V S0) REGULATOR



OCP = R9841 x 8.5uA / R9840
OCP = 14.4A

PCH VCCIO (1.05V) POWER SUPPLY	
Apple Inc.	DRAWING NUMBER 051-9589
NOTICE OF PROPRIETARY PROPERTY:	REVISION 4.18.0
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:	BRANCH
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE	PAGE 98 OF 132
II NOT TO REPRODUCE OR COPY IT	SHEET 87 OF 99
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART	
IV ALL RIGHTS RESERVED	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?
MEM_DQBL2BL	*	16 MILS	?
MEM_DQCH2CH	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER


DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	12 28 29 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	12 28 29 32
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	12 28 29 32
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CS L<3..2>	12 28 32
MEM_A_CNTRL1	MEM_37S	MEM_CTRL	MEM A CS L<1>	12 29 32
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CS L<0>	12 28 32
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A ODT<3..2>	12 29 32
MEM_A_CNTRL1	MEM_37S	MEM_CTRL	MEM A ODT<1>	12 29 32
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A ODT<0>	12 28 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	12 28 29 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM A DQ<7..0>	12 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM A DQ<15..8>	12 28 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM A DQ<23..16>	12 28 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM A DQ<31..24>	12 28 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM A DQ<39..32>	12 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM A DQ<47..40>	12 28 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM A DQ<55..48>	12 28 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM A DQ<63..56>	12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	12 28 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	12 30 31 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	12 30 31 32
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CKE<3..2>	12 30 32
MEM_B_CNTRL1	MEM_37S	MEM_CTRL	MEM B CKE<1>	12 31 32
MEM_B_CNTRL0	MEM_37S	MEM_CTRL	MEM B CKE<0>	12 30 32
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	12 30 31 32
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B ODT<3..1>	12 31 32
MEM_B_CNTRL0	MEM_37S	MEM_CTRL	MEM B ODT<0>	12 30 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..7>	12 30 31 32
MEM_B_CMD6	MEM_40S	MEM_CMD	MEM B A<6>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<5..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	12 30 31 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM B DQ<7..0>	12 30 31
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM B DQ<15..8>	12 30 31
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM B DQ<23..16>	12 30 31
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM B DQ<31..24>	12 30 31
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM B DQ<39..32>	12 30 31
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM B DQ<47..40>	12 30 31
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM B DQ<55..48>	12 30 31
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM B DQ<63..56>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	12 30 31

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
Memory Constraints			
 Apple Inc.	DRAWING NUMBER	051-9589	SIZE D
	REVISION	4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	101 OF 132
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	90 OF 99
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?


SPI Interface Constraints

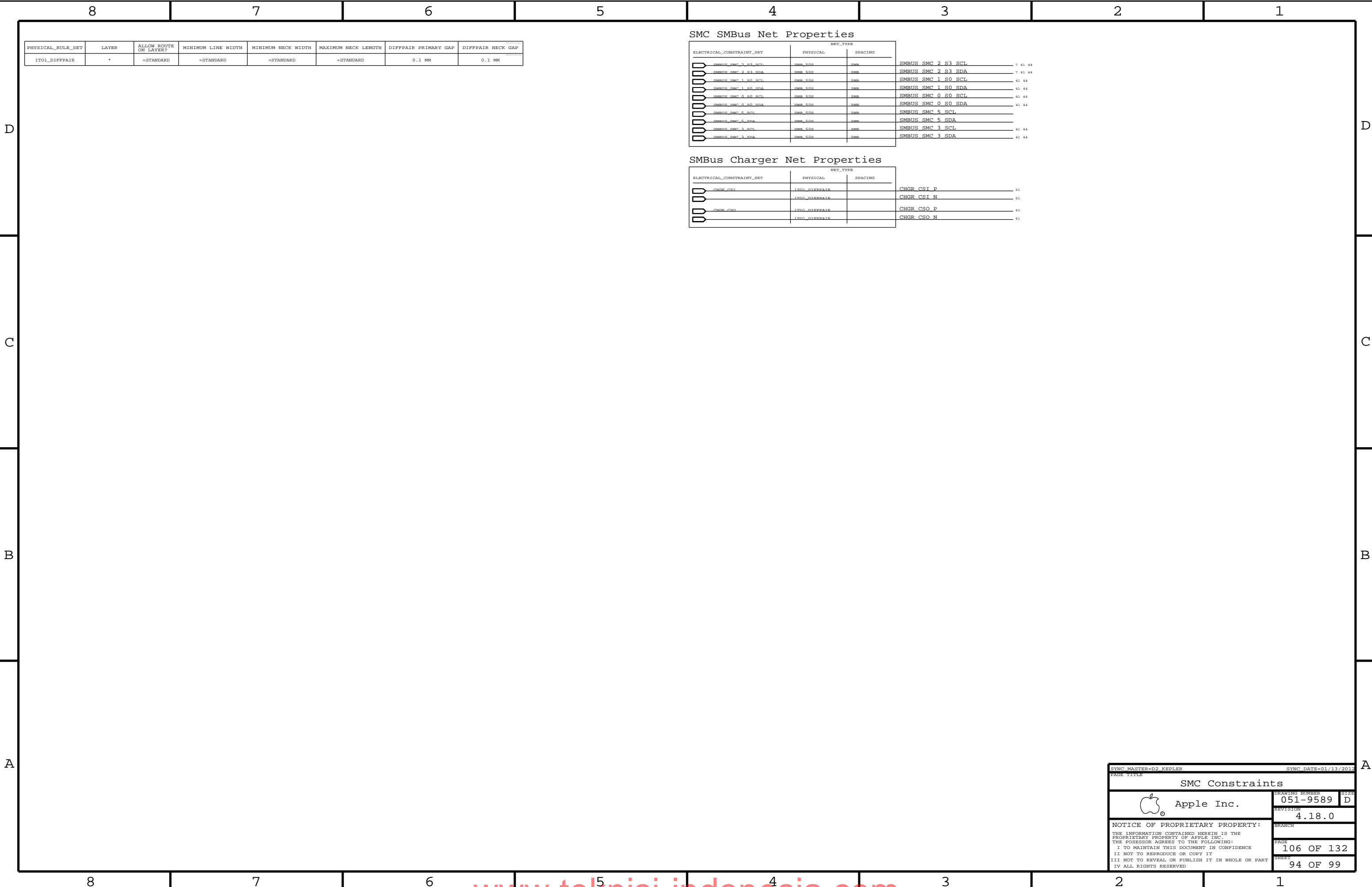
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL		NET_TYPE		SPACING	
	LPC_AD	LPC_508	LPC	LPC_AD<3...0>		7	17 41 43 82
	LPC_FRAME_I	LPC_508	LPC	LPC_FRAME_I		7	17 41 43 82
	LPC_RESET_I	LPC_508	LPC	LPC_RESET_I		25	
	PCF_LPC_CLK0	CLK_LPC_508	CLK_LPC	LPC_CLK33M_SMC_R		19	35
		CLK_LPC_508	CLK_LPC	LPC_CLK33M_SMC		25	41
		CLK_LPC_508	CLK_LPC	LPC_CLK33M_LPCPLUS		7	25 43
	SMBUS_PCH_CLK	SMB_508	SMB	SMBUS_PCH_CLK		17	44
	SMBUS_PCH_DATA	SMB_508	SMB	SMBUS_PCH_DATA		17	44
	SMBUS_PCH_0_CLK	SMB_508	SMB	SMB_PCH_0_CLK		17	44
	SMBUS_PCH_0_DATA	SMB_508	SMB	SMB_PCH_0_DATA		17	44
	SMBUS_PCH_1_CLK	SMB_508	SMB	SMB_PCH_1_CLK		17	44
	SMBUS_PCH_1_DATA	SMB_508	SMB	SMB_PCH_1_DATA		17	44
	HDA_BIT_CLK	HDA_508	HDA	HDA_BIT_CLK		17	53
		HDA_508	HDA	HDA_BIT_CLK_R		17	
	HDA_SYNC	HDA_508	HDA	HDA_SYNC		17	53
		HDA_508	HDA	HDA_SYNC_R		17	
	HDA_RST_I	HDA_508	HDA	HDA_RST_R_L		17	
		HDA_508	HDA	HDA_RST_L		17	53
	HDA_SDIN0	HDA_508	HDA	HDA_SDIN0		17	53
		HDA_508	HDA	AUD_SDI_R		53	
	HDA_SDOUTT	HDA_508	HDA	HDA_SDOUTT		17	53
		HDA_508	HDA	HDA_SDOUT_R		17	25
	SPI_CLK	SPI_508	SPI	SPI_CLK_R		17	43
		SPI_508	SPI	SPI_CLK		43	
	SPI_MOSI	SPI_508	SPI	SPI_MOSI_R		17	43
		SPI_508	SPI	SPI_MOSI		43	
	SPI_MISO	SPI_508	SPI	SPI_MISO		17	43
	SPI_CS0	SPI_508	SPI	SPI_CS0_R_L		17	43
		SPI_508	SPI	SPI_CS0_L		43	
	PCIE_ENET_R2D_P	PCIE_850	PCIE	PCIE_ENET_R2D_P			
		PCIE_850	PCIE	PCIE_ENET_R2D_N			
	PCIE_ENET_R2Dn	PCIE_850	PCIE	PCIE_ENET_R2D_C_P		7	17 38
		PCIE_850	PCIE	PCIE_ENET_R2D_C_N		7	17 38
	PCIE_ENET_D2R	PCIE_850	PCIE	PCIE_ENET_D2R_P		7	17 38
		PCIE_850	PCIE	PCIE_ENET_D2R_N		7	17 38
		PCIE_850	PCIE	PCIE_ENET_D2R_C_P		7	17 38
		PCIE_850	PCIE	PCIE_ENET_D2R_C_N			
	PCIE_AP_R2D_P	PCIE_850	PCIE	PCIE_AP_R2D_P		7	34
		PCIE_850	PCIE	PCIE_AP_R2D_N		7	34
	PCIE_AP_R2Dn	PCIE_850	PCIE	PCIE_AP_R2D_C_P		17	34
		PCIE_850	PCIE	PCIE_AP_R2D_C_N		17	34
	PCIE_AP_D2R	PCIE_850	PCIE	PCIE_AP_D2R_P		17	34
		PCIE_850	PCIE	PCIE_AP_D2R_N		17	34
999	PCIE_AP_D2R	PCIE_850	PCIE	PCIE_AP_D2R_PI_P		7	34
999		PCIE_850	PCIE	PCIE_AP_D2R_PI_N		7	34
999	PCIE_AP_D2R	PCIE_850	PCIE	PCIE_AP_R2D_PI_P		34	
999		PCIE_850	PCIE	PCIE_AP_R2D_PI_N		34	
	PCIE_TBT_D2R	PCIE_850	PCIE	PCIE_SSD_D2R_MUX_OUT_P		39	
		PCIE_850	PCIE	PCIE_SSD_D2R_MUX_OUT_N		39	
	PCIE_TBT_R2Dn	PCIE_850	PCIE	PCIE_SSD_R2D_C_P<1...0>		9	39
		PCIE_850	PCIE	PCIE_SSD_R2D_C_N<1...0>		9	39
	PCIE_TBT_D2R	PCIE_850	PCIE	PCIE_SSD_D2R_P<1...0>		9	39
		PCIE_850	PCIE	PCIE_SSD_D2R_N<1...0>		9	39
	PCIE_TBT_R2D	PCIE_850	PCIE	PCIE_SSD_R2D_MUX_IN_P		39	
		PCIE_850	PCIE	PCIE_SSD_R2D_MUX_IN_N		39	

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE			
PCH Constraints 2			
	Apple Inc.	DRAWING NUMBER	051-9589
		SIZE	D
		REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		103 OF 132	
		SHEET	
		92 OF 99	



PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1To1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	SMBUS_SMC_2_S3_SCL	SMB_50G	SMB	SMBUS_SMC_2_S3_SCL	7 41 44
	SMBUS_SMC_2_S3_SDA	SMB_50G	SMB	SMBUS_SMC_2_S3_SDA	7 41 44
	SMBUS_SMC_1_S0_SCL	SMB_50G	SMB	SMBUS_SMC_1_S0_SCL	41 44
	SMBUS_SMC_1_S0_SDA	SMB_50G	SMB	SMBUS_SMC_1_S0_SDA	41 44
	SMBUS_SMC_0_S0_SCL	SMB_50G	SMB	SMBUS_SMC_0_S0_SCL	41 44
	SMBUS_SMC_0_S0_SDA	SMB_50G	SMB	SMBUS_SMC_0_S0_SDA	41 44
	SMBUS_SMC_5_SCL	SMB_50G	SMB	SMBUS_SMC_5_SCL	
	SMBUS_SMC_5_SDA	SMB_50G	SMB	SMBUS_SMC_5_SDA	
	SMBUS_SMC_3_SCL	SMB_50G	SMB	SMBUS_SMC_3_SCL	41 44
	SMBUS_SMC_3_SDA	SMB_50G	SMB	SMBUS_SMC_3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	CHGR_CSI_P	1TO1_DIFFPAIR		CHGR_CSI_P	61
	CHGR_CSI_N	1TO1_DIFFPAIR		CHGR_CSI_N	61
	CHGR_CSO_P	1TO1_DIFFPAIR		CHGR_CSO_P	61
	CHGR_CSO_N	1TO1_DIFFPAIR		CHGR_CSO_N	61

SYNC MASTER=D2 KEPLER

SYNC DATE=01/13/2012

SMC Constraints

Apple Inc.

DRAWING NUMBER

051-9589

SIZE

D

REVISION

4.18.0

BRANCH

PAGE

106 OF 132

SHEET

94 OF 99

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?	GDDR5_CLK	TOP, BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?	GDDR5_CMD	TOP, BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?	GDDR5_DATA	TOP, BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?	GDDR5_EDC	TOP, BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_8SD	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.

DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.

MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SIGNAL	
NET	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P
NET	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N
NET	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P
NET	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N
NET	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 A<8...0>
NET	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 A<8...0>
NET	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 ABI L
NET	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 ABI L
NET	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 RAS L
NET	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 RAS L
NET	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CAS L
NET	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CAS L
NET	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 WE L
NET	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 WE L
NET	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 CKE L
NET	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 CKE L
NET	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CS L
NET	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CS L
NET	FB_A0_EDC0	GDDR5_45SE	GDDR5_ENC	FB A0 EDC<0>
NET	FB_A0_EDC1	GDDR5_45SE	GDDR5_ENC	FB A0 EDC<1>
NET	FB_A0_EDC2	GDDR5_45SE	GDDR5_ENC	FB A0 EDC<2>
NET	FB_A0_EDC3	GDDR5_45SE	GDDR5_ENC	FB A0 EDC<3>
NET	FB_A1_EDC0	GDDR5_45SE	GDDR5_ENC	FB A1 EDC<0>
NET	FB_A1_EDC1	GDDR5_45SE	GDDR5_ENC	FB A1 EDC<1>
NET	FB_A1_EDC2	GDDR5_45SE	GDDR5_ENC	FB A1 EDC<2>
NET	FB_A1_EDC3	GDDR5_45SE	GDDR5_ENC	FB A1 EDC<3>
NET	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0>
NET	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1>
NET	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2>
NET	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3>
NET	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0>
NET	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1>
NET	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2>
NET	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3>
NET	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0>
NET	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0>
NET	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1>
NET	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1>
NET	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0>
NET	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0>
NET	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1>
NET	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1>
NET	FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<7...0>
NET	FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<15...8>
NET	FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<23...16>
NET	FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<31...24>
NET	FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<7...0>
NET	FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<15...8>
NET	FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<23...16>
NET	FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<31...24>
NET	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 RESET L
NET	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 RESET L











GDDR5 FB B Net Properties


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
FE00	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P
FE00	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N
FE00	FB_B1_CLK	GDDR5_80D	GDDR5_CLK_P	FB_B1_CLK_P
FE00	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L
FE00	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L
FE00	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L
FE00	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>
FE00	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>
FE00	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>
FE00	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>
FE00	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>
FE00	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>
FE00	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>
FE00	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>
FE00	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>
FE00	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>
FE00	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>
FE00	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>
FE00	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>
FE00	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>
FE00	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>
FE00	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>
FE00	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>
FE00	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>
FE00	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>
FE00	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>
FE00	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>
FE00	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>
FE00	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>
FE00	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>
FE00	FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>
FE00	FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>
FE00	FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>
FE00	FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>
FE00	FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>
FE00	FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>
FE00	FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>
FE00	FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>
FE00	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L
FE00	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PIN_7709A		
	DP_85N	DISPLAYPORT	
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML C P<3..0>
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT ML C N<3..0>
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT AUX C P
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT AUX C N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT AUX P
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT EG AUX N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP INT EG AUX P
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML P<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML F P<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT ML F N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT EG ML P<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP INT EG ML N<3..0>
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DPA IG AUX CH P
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DPA IG AUX CH N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DPB IG AUX CH P
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DPB IG AUX CH N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK0 EG AUXCH P
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK0 EG AUXCH N
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK1 EG AUXCH P
DP_INT_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK1 EG AUXCH N
TBT_A_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK0 AUXCH C P
TBT_B_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK0 AUXCH C N
TBT_C_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK1 AUXCH C P
TBT_D_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK1 AUXCH C N
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK0 ML C P<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK0 ML C N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK1 ML C P<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK1 ML C N<3..0>
TBT_A_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK0 AUXCH P
TBT_B_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK0 AUXCH N
TBT_C_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK1 AUXCH P
TBT_D_AUXCH	DP_85N	DISPLAYPORT	DP TBSNK1 AUXCH N
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK0 ML P<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK0 ML N<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK1 ML P<3..0>
DP_INT_ML	DP_85N	DISPLAYPORT	DP TBSNK1 ML N<3..0>

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET		REF_TYPE		
		PROBABLE	DEFINITION	
	GPU_CLK27M	CLK_STROM_55R	CLK_STROM	GPU OSC 27M XTALIN 77 78
	GPU_CLK27M	CLK_STROM_55R	CLK_STROM	GPU OSC 27M XTALOUT 77 78
	GPU_CLK27M	CLK_STROM_55R	CLK_STROM	GPU OSC 27M XTAL BUFFOUT 77 78
	GPU_CLK27M	CLK_STROM_55R	CLK_STROM	GPU OSC 27M SSIN 77 78
		1:1 DIEREPAIR		PEX TSTCLK O P 71 92
		1:1 DIEREPAIR		PEX TSTCLK O N 71 92
	HDMI_DATA	HDMI_00D	HDMI1	HDMI EG DATA C P<2..0> 7 38
		HDMI_00D	HDMI1	HDMI EG DATA C N<2..0> 7 38
	HDMI_CLK	HDMI_00D	HDMI1	HDMI EG CLK_C_P 7 38
		HDMI_00D	HDMI1	HDMI EG CLK_C_N 7 38

SYNC MASTER=D2 KEPLER		SYNC DATE=01/13/2012	
PAGE TITLE		PAGE NO	
GPU (Kepler) CONSTRAINTS			
 Apple Inc.		DRAWING NUMBER	D
		051-9589	
		REVISION	
		4.18.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		107 OF 132	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		95 OF 99	
IV ALL RIGHTS RESERVED			

D

CBA

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.


8

5 1 4

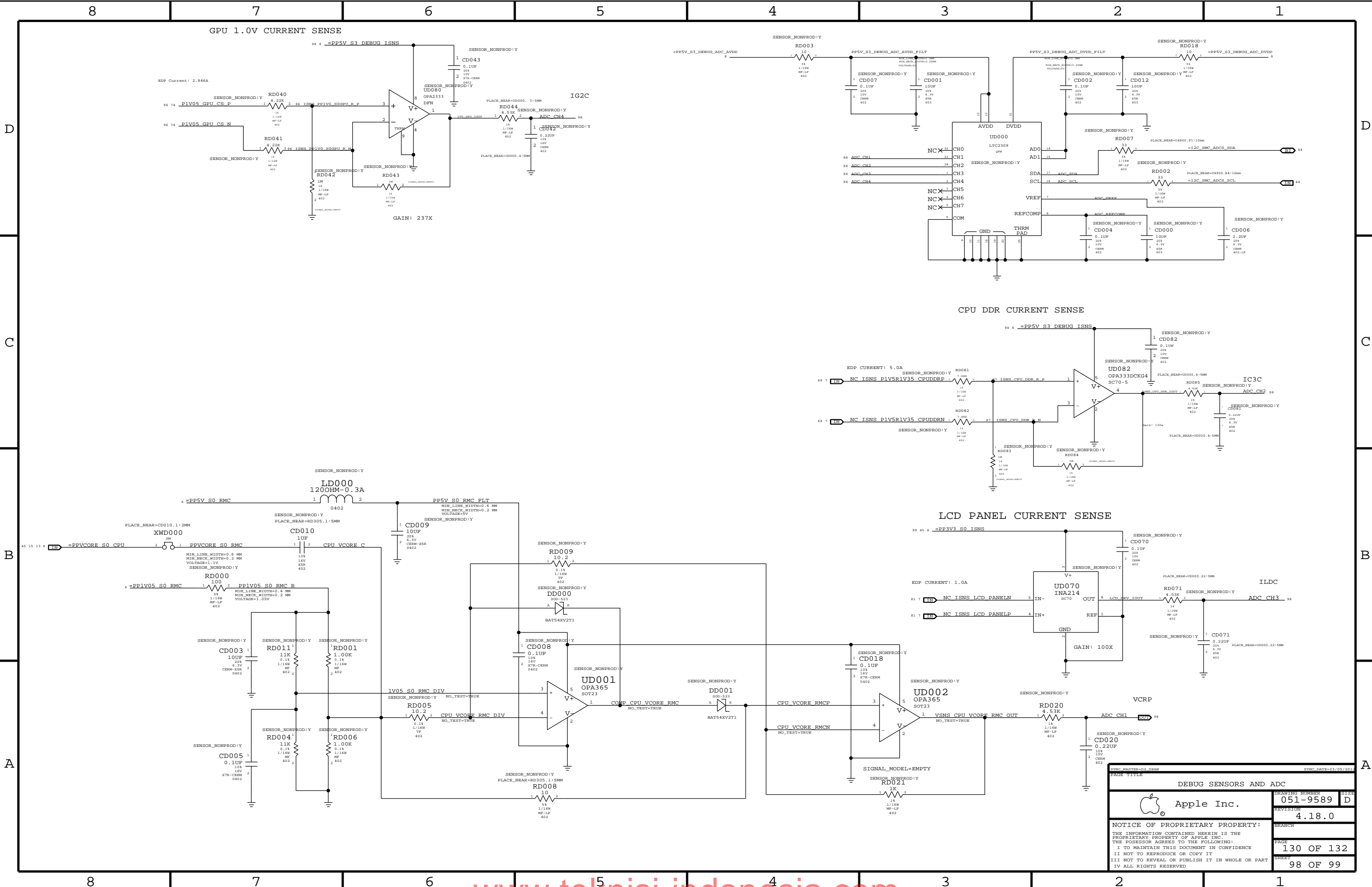
4


SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

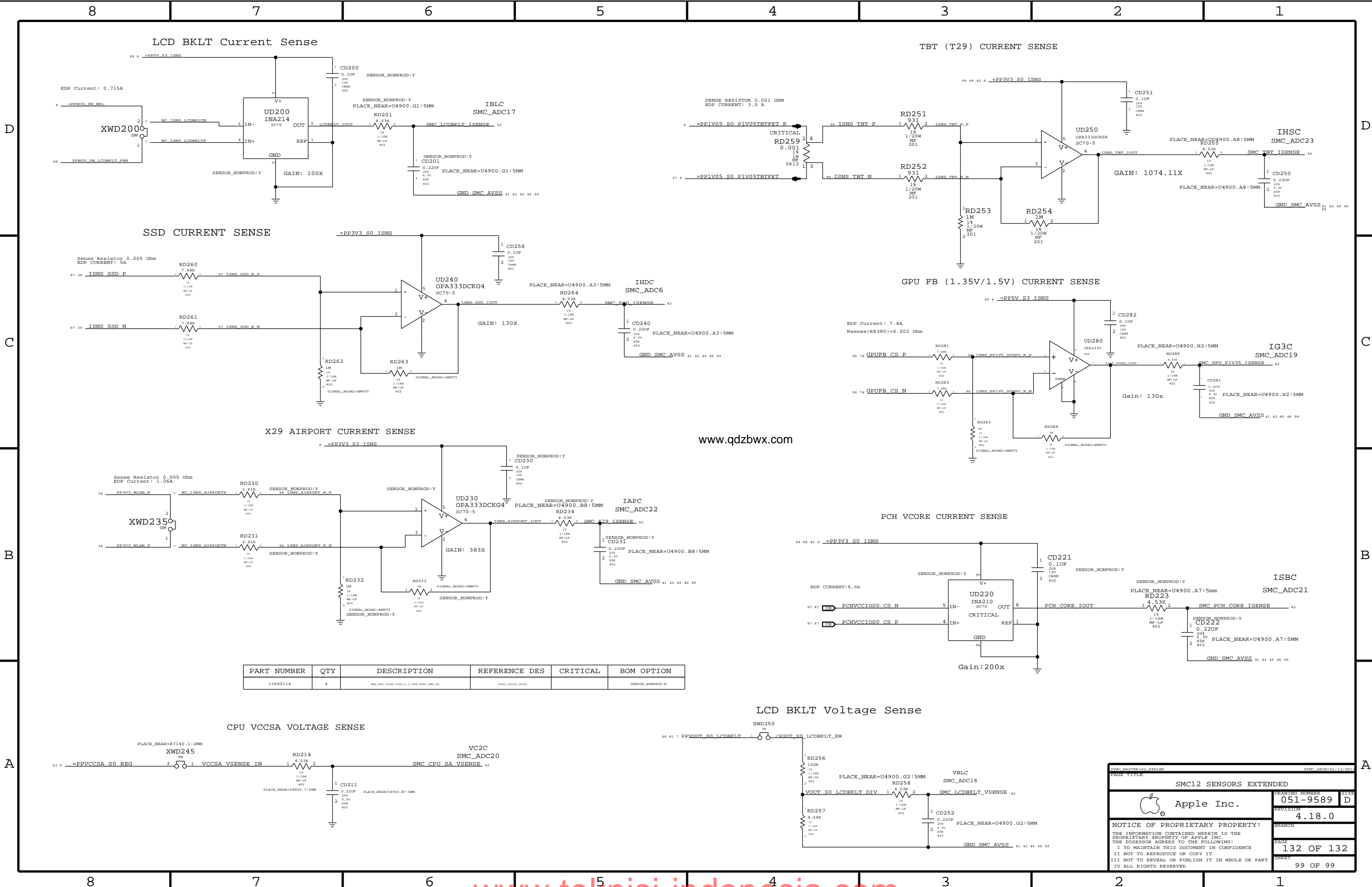
PAGE TITLE
PCB Rule Definitions

	Apple Inc.	DRAWING NUMBER		SIZE	
		051-9589		D	
		REVISION			
		4.18.0			
NOTICE OF PROPRIETARY PROPERTY:				BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE FORSOWNER AGREES TO THE FOLLOWING:				PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART ALL RIGHTS RESERVED				109 OF 132	
				SHEET	
				97 OF 99	


III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 IV ALL RIGHTS RESERVED



PAGE TITLE		SYMC DATE=03/05/2015
DEBUG SENSORS AND ADC		
 Apple Inc.	DRAWING NUMBER	051-9589
	REVISION	4.18.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH	
	PAGE	130 OF 132
	SHEET	98 OF 99



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	4	R402, RFL, 100K, 5, 1/16W, 0402, SMD, LF	CD201, CD222, CD231		SENSOR_NONPROD:N

SYMC MASTER-02 KEYFILE		SYMC DATE=01/13/2015	
PAGE TITLE			
SMC12 SENSORS EXTENDED			
	DRAWING NUMBER		SHEET
	051-9589		D
	REVISION		
	4.18.0		
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
PAGE		132 OF 132	
SHEET		99 OF 99	